JTE HCM-UTE
ISSN: 2615-9740

JOURNAL OF TECHNICAL EDUCATION SCIENCE
Ho Chi Minh City University of Technology and Engineering
Website: https://jte.edu.vn
Email: jte@hcmute.edu.vn

Design and Performance Evaluation of SRAM Processing in Memory Using TSMC 90nm CMOS Technology

Thanh-Trung Vu, Tuan-Khuong Bui, Duc-Huy Hoang, Van-Khoa Pham*
Ho Chi Minh City University of Technology and Engineering, Vietnam

*Corresponding author. Email: khoapv@hcmute.edu.vn

ARTICLE INFO

Received: 17/01/2025
Revised: 13/02/2025
Accepted: 03/03/2025
Online First: 18/09/2025
Published: 28/08/2026

KEYWORDS

Static random-access memory;
8T-SRAM cell design;
SRAM processing on memory;
8T-SRAM processing on memory;
Power consumption.

ABSTRACT

Memory is a crucial component in electronic circuits, especially in embedded devices. With the rapid development of AI and Machine Learning, the demand for processing large amounts of data has exposed the limitations of CPUs and the high costs of GPUs. The Processing-In-Memory (PIM) architecture addresses the bottleneck issue by integrating processing capabilities directly into memory. Static random-access memory (SRAM), a high-speed memory type, is commonly used as cache and main memory in CPUs. Integrating processing directly into SRAM, SRAM-based processing in memory enhances performance and alleviates bottleneck problems. In this study, the design and evaluation of two 64-bit SRAM Processing-In-Memory architectures were implemented on TSMC's 90nm technology using Cadence Virtuoso software. Computational operations, such as ternary multiplication, were simulated and analyzed its power consumption under PVT conditions evaluate the stability and accuracy. The research results provide a deeper understanding of SRAM-based in-memory processing design, improve knowledge and skills in circuit design, and propose further developments for SRAM Processing-In-Memory in the future.

DOI: https://doi.org/10.54644/jte.2025.1797

1. Introduction

In the last decades, there has been an enormous demand for processing large amounts of information with low latency and high-energy efficiency. Especially, CMOS microchip technology has made significant contributions to the development of the semiconductor manufacturing industry [1]. In the memory hierarchy architecture of most modern computers, the cache, due to its proximity to the processor, plays a crucial role in improving system performance. However, the traditional Von-Neumann architecture has a major challenge: the bottleneck between memory and the processor caused by the continuous movement of data back and forth [1]-[3]. To solve this limitation, the Processing-In-Memory (PIM) architecture was introduced, representing a breakthrough by integrating processing capabilities directly into the memory. The PIM architecture, especially designs utilizing SRAM, not only stores data but also performs computations in place. This significantly reduces latency and energy consumption while accelerating system operations [4]-[6]. Nowadays, with the evolution in the field of artificial intelligence (AI), the PIM memory, with its outstanding advantages, is becoming an ideal solution. It overcomes the limitations of the Von-Neumann architecture and opens up new opportunities for optimizing modern microchip designs [7]. The diagram in figure 1 can illustrate how the PIM structure differs from traditional Von-Neumann architecture.

JTE
HCM-UTE
ISSN: 2615-9740

JOURNAL OF TECHNICAL EDUCATION SCIENCE
Ho Chi Minh City University of Technology and Engineering
Website: https://jte.edu.vn
Email: jte@hcmute.edu.vn

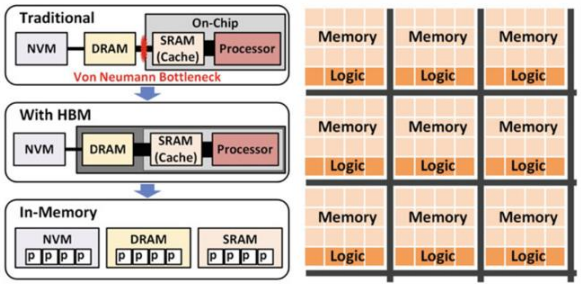

Figure 1. *The difference of Von-Neumann and PIM architecture [7].*

2. Methods

This study applies the principle of the conventional 6T SRAM cell to design and extend two types of 8T SRAM-based Processing-In-Memory (PIM) architectures using the 90-nm CMOS technology. Both designs preserve the standard read/write operations of the 6T SRAM while introducing additional functionality for in-memory multiplication. The proposed designs were first implemented and validated at the single-bit cell level to verify correct read/write and multiplication operations. Subsequently, the two architectures were extended to a 64-bit SRAM array to examine scalability and functional stability under parallel operations. Then the power consumption which were analyzed under Process, Voltage, and Temperature (PVT) variations across a frequency range of 100 MHz was conducted to observe variation trends and to assess the stability of the designs under different operating conditions.

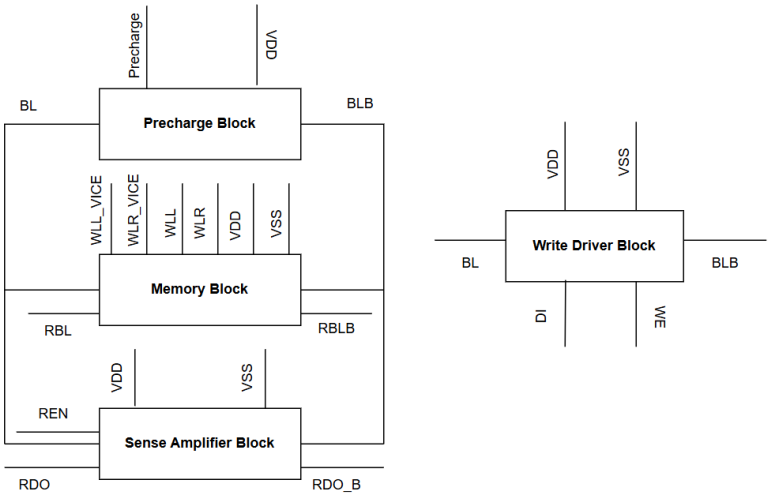

Figure 2. *Block diagram of execution of data write/read operation to SRAM PIM memory cell [10].*

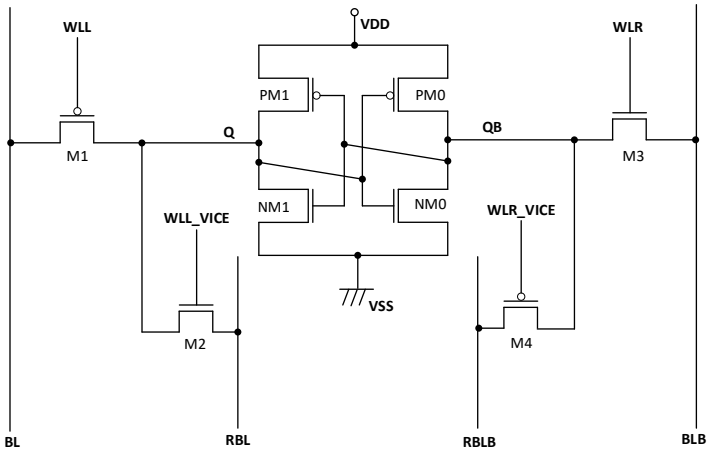

Figure 3. *SRAM PIM memory cell design with four WL lines.*

The SRAM PIM memory is composed of an array of memory cells combined with various peripheral blocks. The main peripheral blocks include the column decoder, row decoder, sense amplifier, write driver, precharge block, and memory block. These blocks work together to ensure the ability to read/write data and perform ternary computation processing in memory. Figure 2 illustrates the block diagram of SRAM memory. The blocks in the system are interconnected via the BL and BLB lines, while VDD and VSS serve as the power supply for the entire system. The precharge block precharges the BL and BLB lines to a voltage approximately equal to VDD. The write driver block outputs the BL and BLB values when triggered by the DI and WE signals. The sense amplifier block amplifies the value stored in the memory cell when the REN signal is active; at this point, the RDO signal represents the amplified data from the memory cell. The memory block is responsible for storing, writing, and reading data, as well as performing logical operations.

The SRAM PIM design features four WL lines [8], similar to a standard SRAM design, consisting of four transistors forming two NOT gates. Transistors M1 and M3 are controlled by two write signals, WLL and WLR, which enable connections between nodes Q and QB with the BL and BLB lines. The other two transistors, M2 and M4, are controlled by read access signals WLL_VICE and WLR_VICE, allowing the sense amplifier to read data from the SRAM. Two additional signal lines, RBL and RBLB, are used to read data from the SRAM memory cell. The proposed design is shown in Figure 3.

The SRAM PIM design with the RWL line [9] includes 8 transistors, of which 6 transistors are designed as a standard 6T SRAM, and 2 additional NMOS transistors are used for reading, connecting RWL with Q and QB. The proposed design is illustrated in Figure 4.

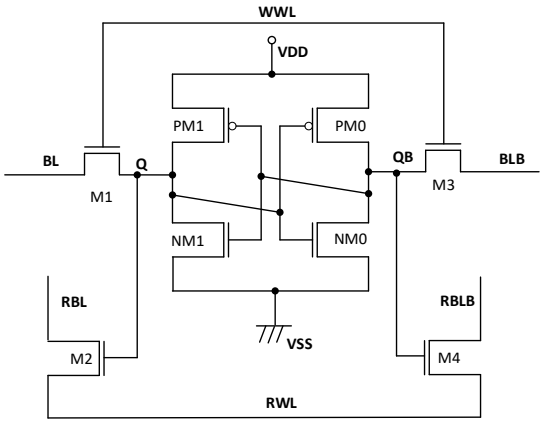

Figure 4. *Design of SRAM PIM memory cell with RWL line.*

First, the read/write functionality is discussed. At this time, the BL and RBL lines are not connected, and similarly, the BLB and RBLB lines are also not connected. The central block, the SRAM block, is responsible for performing the main functions, including writing data from DI and correctly reading back the written value. The precharge block, when the PRE signal = 0, sets the BL and BLB lines to the same voltage level of 0.5VDD. This process occurs before the data writing operation. The write block directly connects to the BL and BLB lines to write the value corresponding to DI into the SRAM. The sense amplifier is responsible for amplifying the value stored in the memory cell at nodes Q and QB and displaying the output values through the RDO and RDO_B lines. The VDD and VSS power supplies provide fixed values to the blocks, while the signal lines use pulse voltage blocks with timing adjusted to suit the entire system.

Next, the ternary multiplication function is activated. At this point, the BL and RBL lines are connected, and similarly, the BLB and RBLB lines are also connected through a tristate gate. The 8T SRAM block can now perform ternary multiplication. The principle of this multiplication involves X × W. The value of X is represented through the four WL lines, while W is represented by Q and QB. The

value of W is determined by the value stored at nodes Q and QB: if Q = 1 and QB = 0, then W = 1; conversely, if Q = 0 and QB = 1, then W = -1. These values are summarized in Table 1 [8].

Table 1. *Values of weight W.*

Q	QB	W
1	0	1
0	1	-1

For the value of X, it is adjusted through the four WL lines. The ternary multiplication operation corresponds to three values of X, which are X = 1, X = -1, and X = 0. To generate these X values, we refer to Table 2 [8], which summarizes the possible configurations of the WL lines.

Table 2. *Values of X.*

WLL	WLL_VICE	WLR	WLR_VICE	X
1	0	1	0	-1
1	0	0	1	0
0	1	0	1	1

The result of the ternary multiplication is based on the voltage changes of BL and RBL, as well as BLB and RBLB. When the operation is performed, the voltage values on these lines will change correspondingly, as summarized in Table 3 [8].

Table 3. *Result of ternary multiplication.*

X	W	Result
-1	-1	BLB/RBLB are charged to correspond ΔV = +1
-1	1	BLB/RBLB are discharged to correspond ΔV = -1
1	-1	BL/RBL are discharged to correspond ΔV = -1
1	1	BL/RBL are charged to correspond ΔV = +1
0	-1 and 1	No charge/discharge

The operation principle of the SRAM PIM design with the RWL line shown in Figure 4 is as follows: A value of '0' or '1' is assigned to the RWL input by applying a high voltage and a short negative pulse. On the other hand, the weight is stored in the memory cell as '-1' (i.e., Q = H, QB = L) or +1 (i.e., Q = 0, QB = 1), based on the internal voltage stored in the SRAM bit-cell. The states of the input combinations and weights are shown in Table 4. When RWL is at a high voltage (H), no current flows through the two additional NMOS transistors, and thus VRBL - VRBLB = 0. When a short negative pulse is applied to RWL, one of the two NMOS transistors (i.e., the transistor with its gate connected to a high storage node) turns on and is used to discharge one of the read bit-lines, RBL (resulting in VRBL - VRBLB = -1) or RBLB (resulting in VRBL - VRBLB = +1) [9].

Table 4. *Input value and storage weight.*

DI	RWL	RBL	RBLB	VOUT	S(sign)
Q=0,QB=1 (+1)	0(1)	1	0	1	0(+)
Q=1,QB=0 (-1)	0(1)	0	1	1	1(-)
Q=0,QB=1 (+1)	1(0)	1	1	0	0(+)
Q=1,QB=0 (-1)	1(0)	1	1	0	0(+)

JTE
HCM-UTE
ISSN: 2615-9740

JOURNAL OF TECHNICAL EDUCATION SCIENCE
Ho Chi Minh City University of Technology and Engineering
Website: https://jte.edu.vn
Email: jte@hcmute.edu.vn

3. Results

3.1. Simulation results of Processing-In Memory SRAM design with four Word-Lines

In stage A, at time t = 4ns, after WLL and WLR are activated, the input data DI = 0 and WE is activated to a high level. Therefore, the value of Q = 0 and QB = 1, successfully write the value into the memory cell. Then, in stage B, WLL and WLR are activated again, and the REN signal is turned on to read data from the memory cell. As a result, RDO is 0 and RDO_B is 1. In stage C, at time t = 24ns, the input data DI = 1 and WE is activated to write data into the memory cell. Therefore, the value of Q = 1 and QB = 0. In stage D, both WL signals are activated again, and the REN signal is turned on to read data from the memory cell. As a result, RDO is 1. These stages are illustrated in Figure 5, with the input data DI = 0 in the first stage at time t = 4ns and input data DI = 1 in the second stage at t = 24ns.

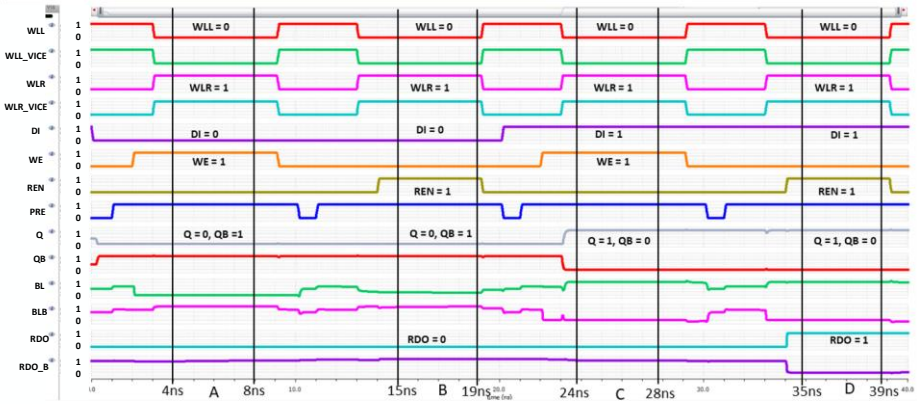

Figure 5. *SRAM PIM write/read process with four WL lines.*

Ternary multiplication operation: First, let's consider the case where X = -1. In this case, the WLL and WLR lines will be at a high level, and the WLL_VICE and WLR_VICE lines will be at a low level. Next, we consider W. Looking at Figure 6, in period A, at time t = 4ns, we see that the input data DI = 1, and at this point, the value at the node Q = 1, QB = 0, corresponding to the value W = 1. In stage B, at t = 14ns, the four WL lines are activated similarly to stage A, and at this point, the REN signal = 1, signaling that the reading process has begun. During this stage, we see that BLB and RBLB discharge the voltage to a level of ΔV = -1. Then, in stages C and D, in stage C at t = 23ns, the WLL, WLL_VICE, WLR, and WLR_VICE signal lines are still set for X = -1. At this point, the input data DI = 0, and the values at node Q and QB are Q = 0 and QB = 1, which represents W = -1. Afterward, in stage D, at t = 34ns, the REN signal is set high. The data stored at Q and QB will be read out at RDO = 0. The result of the ternary multiplication between X and W will be represented at BLB and RBLB, and at this point, both signal lines will be charged to ΔV = +1.

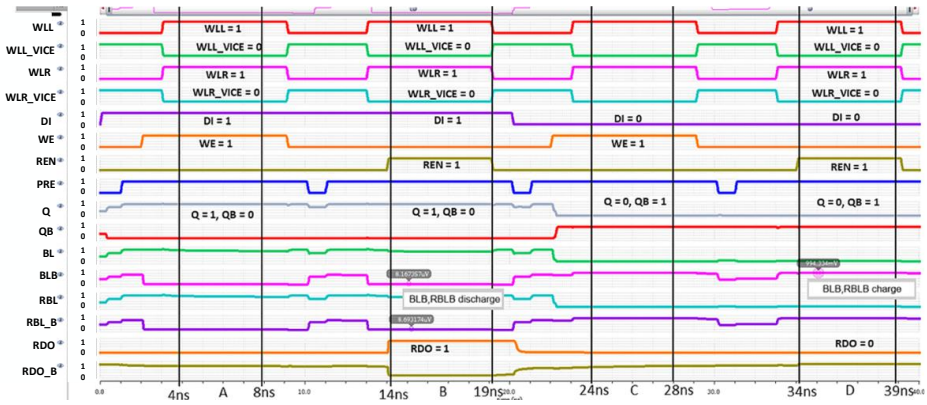

Figure 6. *Waveforms of BL and BLB lines for X = -1 case of SRAM PIM with four WL lines.*

JTE
HCM-UTE
ISSN: 2615-9740

JOURNAL OF TECHNICAL EDUCATION SCIENCE
Ho Chi Minh City University of Technology and Engineering
Website: https://jte.edu.vn
Email: jte@hcmute.edu.vn

The next multiplication discussed is the multiplication with X = 1, and the waveform for this case can be seen in Figure 7. In this case, the WL lines are set as in Table 2. Thus, WLL = 0, WLL_VICE = 1, WLR = 0, and WLR_VICE = 1. In stage A, at t = 4ns, DI = 1 and WE = 1, so Q = 1 and QB = 0, corresponding to the value W = 1, which has been set. Then, in stage B, at t = 14ns, when REN is raised to a high level, the output signal at RDO = 1 is received. At this point, BL and RBL are charged to ΔV = +1, reflecting the result of the multiplication X × W. In stage C, at t = 23ns, the four WL lines remain set with values corresponding to X = 1. At this point, the input data DI = 0, and we get Q = 0 and QB = 1, meaning W = -1. The result of this multiplication is shown in stage D at t = 34ns, where REN = 1 and RDO drops to 0, and the values of BL and RBL discharge to a voltage level of ΔV = -1.

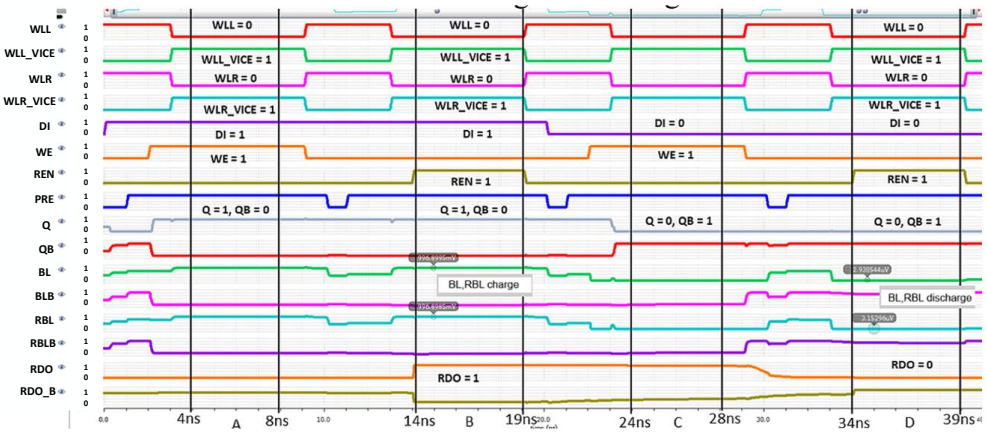

Figure 7. *Waveforms of BL and BLB lines for X = 1 case of SRAM PIM with four WL lines.*

In the final case, when X = 0, all four WL lines are turned off, which corresponds to the opposite state where all four WL lines remain on. Figure 8 illustrates the waveform of the multiplication process for X = 0 and W = -1. In this case, because W = -1, we have Q = 0 and QB = 1, which corresponds to writing DI = 0. Then, at t = 14ns, when the REN signal is set to 1, the correct value is not received at RDO because neither BL nor BLB charges or discharges. At this point, BL and BLB reflect the result of the calculation X × W, and the result of ΔV is approximately 0. In stage D, after all four WL lines are turned back on and the REN signal is set to 1 at t = 34ns, RDO reads the value of Q from stages A and B. This happens because at stage C, the writing process was unsuccessful as all four WL lines remained off at that time.

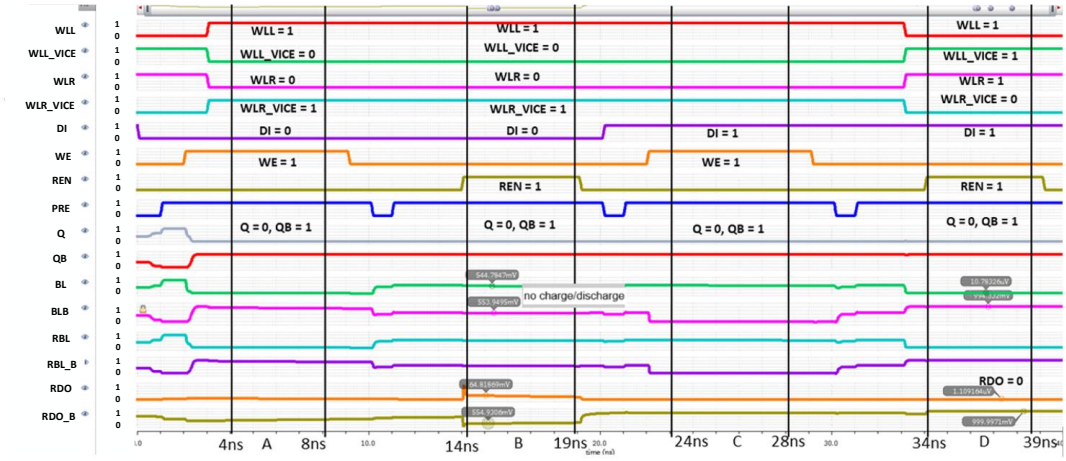

Figure 8. *Waveforms of BL and BLB lines with X = 0, W = -1 case of SRAM PIM with four WL lines.*

JTE HCM-UTE
ISSN: 2615-9740
JOURNAL OF TECHNICAL EDUCATION SCIENCE
Ho Chi Minh City University of Technology and Engineering
Website: https://jte.edu.vn
Email: jte@hcmute.edu.vn

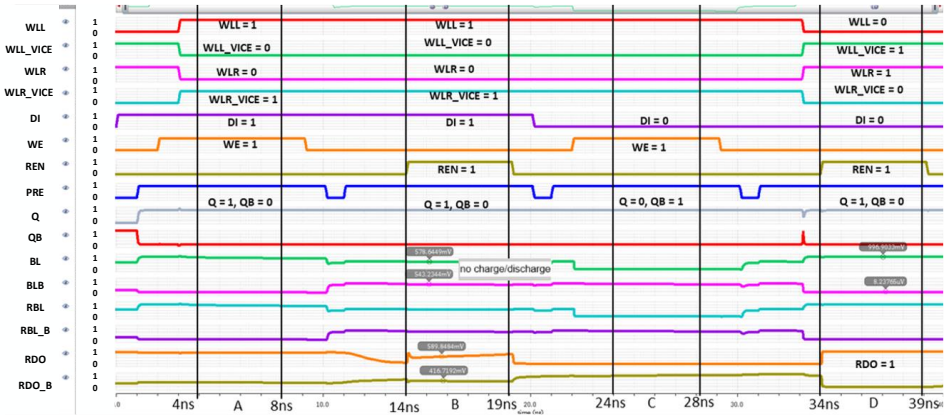

Figure 9. *Waveforms of BL and BLB lines for X = 0, W = 1 case of SRAM PIM with four WL lines.*

Figure 9 illustrates the waveform for the case of multiplication X = 0 and W = 1, we have Q = 1 and QB = 0, which corresponds to writing DI = 1. The process is similar to the multiplication between X = 0 and W = -1. At the t = 14ns, when the REN signal is activated, the RDO signal cannot present the correct value since neither BL nor BLB is charged or discharged, reflecting a voltage level of ΔV that is approximately 0.

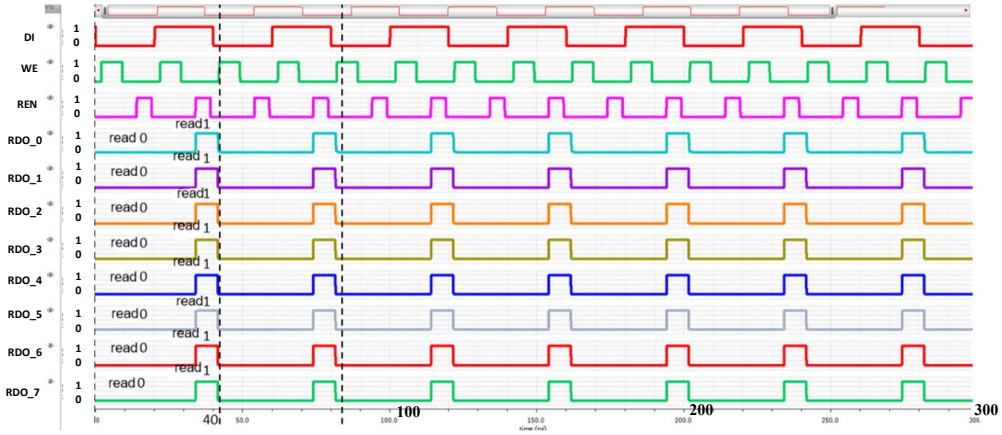

Figure 10. *Waveform showing read/write value of SRAM PIM 64-bit array with four WL lines.*

The simulation results of the 64-bit SRAM Processing-in-Memory array with four WL lines are shown in Figure 10, illustrating the read/write functionality. The output waveform of the first 8 bits of the array during the time interval from 0ns to 40ns demonstrates the RDO signal, reflecting the read results from the SRAM after writing 0 and 1. Subsequently, in the time interval from 40ns to 320ns, the signals represent the results for the subsequent rows in this design.

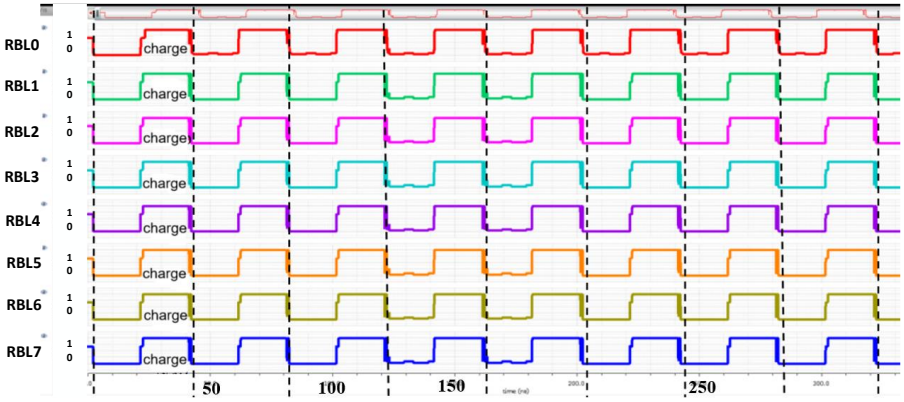

Figure 11. *Output waveform of SRAM PIM 64-bit array with four WL lines in case X = 1.*

JTE
HCM-UTE
ISSN: 2615-9740

JOURNAL OF TECHNICAL EDUCATION SCIENCE
Ho Chi Minh City University of Technology and Engineering
Website: https://jte.edu.vn
Email: jte@hcmute.edu.vn

For the ternary multiplication function, Figure 11 shows the result of the multiplication X = 1 with W = 1 on the lines RBL0 – RBL7, where ΔV = +1 is observed. During the time interval from 20ns to 40ns, the results of the first row in the memory are displayed, while the time interval from 40ns to 320ns shows the results of the remaining rows in this 64-bit array.

The result of multiplying X = -1 by W = 1 is also represented similarly on signals RBLB0 to RBLB7 on the 64-bit array.

3.2. Simulation results of SRAM Processing-In Memory design with Read Word-Line

Figure 12 shows the waveform of the write/read process and the multiplication between the RWL input and the storage weight of the SRAM PIM with the RWL line. In the case of t = 2ns, WE = 1, the start of the write allows DI = 1 to BL which will be 1 and BLB will be 0. At t = 3ns, WWL = 1 allows writing from BL, BLB to the value of Q = 1, QB = 0 and RBL = 1, RBLB = 1, if RWL = 1 then the output value is 0 (i.e. the Vout value = 0 and the + sign is equivalent to S = 0) and at t = 13ns, RWL = 0 then RBL will be discharged to 0 and the VRBL - VRBLB output value will be -1 (i.e. the Vout value = 1 and the - sign is equivalent to S = 1). In case t = 22ns, WE = 1 starts to allow DI = 0 to write to BL will be 0 and BLB will be 1. At t = 23ns, WWL = 1 allows writing from BL and BLB to Q = 0, QB = 1 and RBL = 1, RBLB = 1, if RWL = 1 then the output value is 0 and at t = 33ns, RWL = 0 then RBLB will be discharged to 0 and the output value VRBL - VRBLB will be +1 (i.e. Vout value = 1 and + sign is equivalent to S = 0).

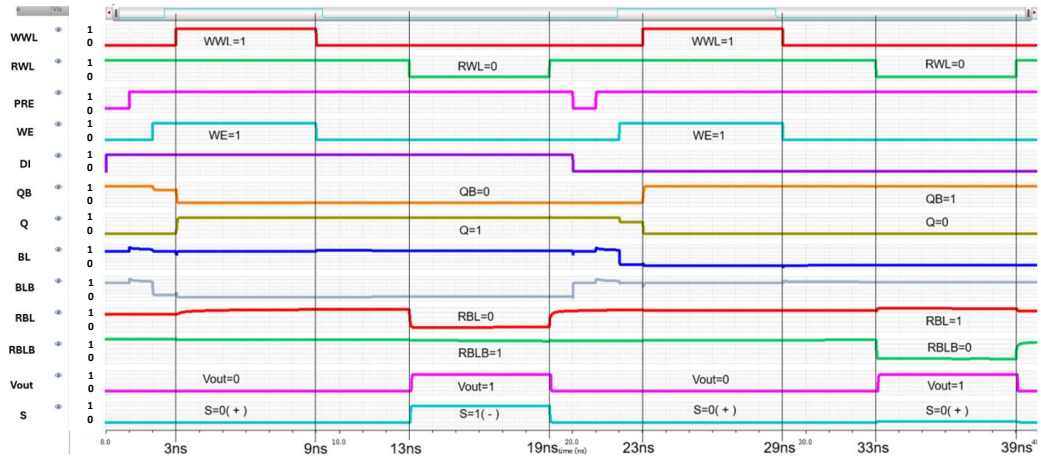

Figure 12. *Waveform of a PIM SRAM memory cell with RWL line.*

Figure 13 shows the output waveform of the first 8-bit row in the 64-bit array in order from Vout0 to Vout7 with sign signals from S0 to S7 and takes place in 40ns.

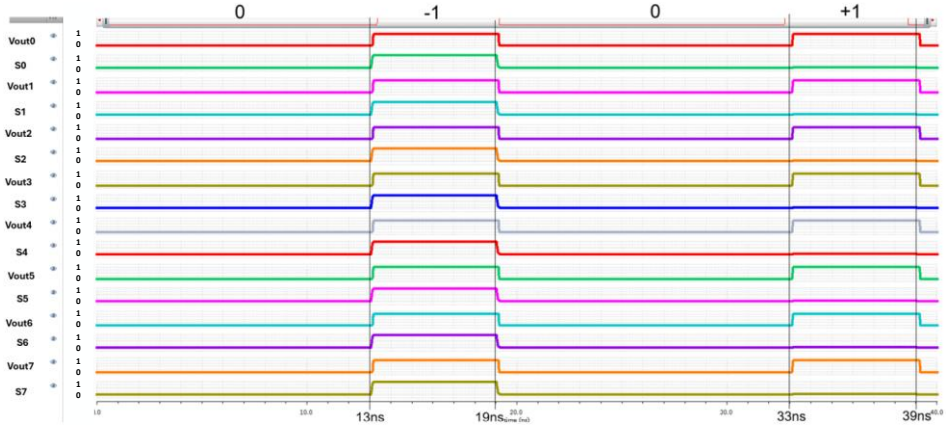

Figure 13. *Output waveform of the first row in a 64-bit PIM SRAM array with RWL line.*

JTE
HCM-UTE
ISSN: 2615-9740

JOURNAL OF TECHNICAL EDUCATION SCIENCE
Ho Chi Minh City University of Technology and Engineering
Website: https://jte.edu.vn
Email: jte@hcmute.edu.vn

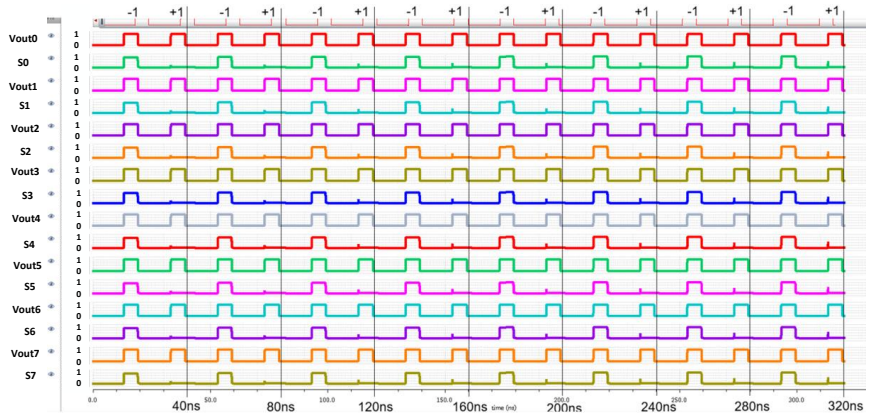

Figure 14. *Output waveform of 64-bit PIM SRAM array with RWL line.*

Figure 14 shows the output waveform of the first 8-bit row in the 64-bit array similar to figure 13 for the period from 0ns to 40ns. Next in the period from 40ns to 80ns is the output waveform of the second 8-bit row and similarly with a period of 40ns until the period from 280ns to 320ns is the output waveform of the last 8-bit row in the 64-bit array.

3.3. Effect of temperature, voltage on the performance of both Processing-In Memory SRAM designs

The PVT (Process, Voltage, Temperature) are important factors that can affect the performance and power consumption of integrated circuit designs such as SRAM PIM with RWL and SRAM PIM with four WL lines. Based on data from a memory cell and a 64-bit array, the following analysis provides a clearer insight into the relationship between PVT and the interactions between these factors.

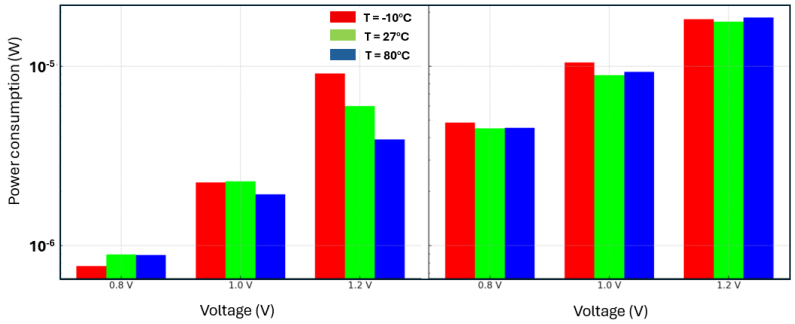

Figure 15. *Graph comparing the average power of two SRAM PIM designs on a single memory cell.*

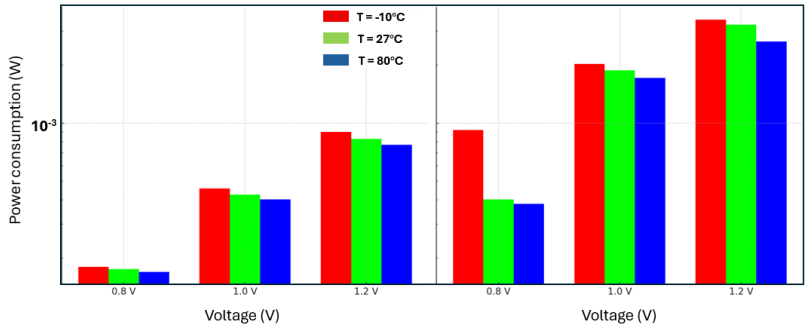

Figure 16. *Graph comparing the average power of two SRAM PIM designs on a 64-bit array.*

Figures 15 and 16 is average power of two SRAM PIM designs which the SRAM PIM with RWL is on the left and the SRAM PIM with four Word-Lines is on the right. It can be seen that the power consumption increases with the square of the voltage ($P \propto V^2$). In the SRAM PIM design with the RWL line, it can be observed that with a single memory cell, at T = 27°C, power increases from 8.9E-7W

(VDD = 0.8V) to 6.00E-6W (VDD = 1.2V), a nearly 7-fold increase. For the 64-bit array at T = 27°C, power increases from 1.7E-4W (VDD = 0.8V) to 8.3E-4W (VDD = 1.2V), a nearly 4.7-fold increase. For the SRAM PIM design with four WL lines, the power for a single memory cell at T = 27°C increases from 4.5E-6W (VDD = 0.8V) to 1.8E-5W (VDD = 1.2V). When simulating with a 64-bit array for this design at T = 27°C, power increases from 4E-4W (VDD = 0.8V) to 3.2E-3W (VDD = 1.2V), a nearly 8-fold increase. This highlights the significant impact of voltage on power consumption.

This section also analyzes the effect of temperature on power consumption. For the SRAM PIM design with the RWL line, power consumption decreases as the temperature increases. For instance, in the single memory cell design at 1.2V, power decreases from 9.1E-6W (T = -10°C) to 3.9E-6W (T = 80°C). Similarly, in the simulation of this design with the 64-bit array at 1.2V, power decreases from 8.9E-4W (T = -10°C) to 7.7E-4W (T = 80°C). For the SRAM PIM design with four WL lines, power consumption is more stable. For example, in the single memory cell design at VDD = 1.2V, power fluctuates from 1.8E-5W (T = -10°C) to 1.9E-5W (T = 80°C). Similarly, in the 64-bit array, at VDD = 1.2V, power fluctuates from 3.4E-3W (T = -10°C) to 2.7E-3W (T = 80°C). The results show that the design with the RWL line reduces power at higher temperatures, while the design with four WL lines is more stable in terms of power consumption.

4. Conclusions

This study has demonstrated the basic operations including write, read, and ternary processing on memory with both SRAM PIM designs using four WL lines and SRAM PIM using the RWL line. The choice between these two designs depends on the application requirements: If energy saving and operation in high-temperature environments are needed, the SRAM PIM with the RWL line design is the optimal choice. If higher stability and reliability are required regardless of temperature and voltage, the design with four WL lines is the more suitable solution. However, in practice, circuit designs often combine the best of both factors to achieve a balance between energy performance and stability. The analysis of the impact of variations in supply voltage and operating temperature on power consumption for write, read, and ternary processing operations on memory has been specifically discussed in this study.

Conflict of Interest

The authors declare no conflict of interest.

REFERENCES

[1] N. H. E. Weste and D. M. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th ed. Boston, MA, USA: Addison-Wesley, 2010.
[2] W. Stallings, *Computer Organization and Architecture: Designing for Performance*, 10th ed. Boston, MA, USA: Pearson, 2016.
[3] M. Qazi, M. E. Sinangil, and A. P. Chandrakasan, "Challenges and directions for low-voltage SRAM," *IEEE Des. Test Comput.*, vol. 28, no. 1, pp. 32–43, 2011.
[4] C. Nie *et al.*, "VSPIM: SRAM processing-in-memory DNN acceleration via vector-scalar operations," *IEEE Trans. Comput.*, vol. 73, no. 10, pp. 2378–2390, Oct. 2024.
[5] K. Yoshioka, S. Ando, S. Miyagi, Y. C. Chen, and W. Zhang, "A review of SRAM-based compute-in-memory circuits," *arXiv preprint arXiv:2411.06079v2*, Nov. 2024.
[6] K. Monga, S. Behera, N. Chaturvedi, and S. Gurunarayanan, "Design of in-memory computing enabled SRAM macro," in *Proc. IEEE 19th India Council Int. Conf. (INDICON)*, Kochi, India, 2022, pp. 1–6.
[7] J. Y. Kim, B. Kim, and T. T. H. Kim, *Processing-in-memory for AI from circuits to systems*, Springer, 2023.
[8] J. Zhang, Z. Lin, X. Wu, C. Peng, W. Lu, Q. Zhao, and J. Chen, "An 8T SRAM array with configurable word lines for in-memory computing operation," 2023, doi: https://doi.org/10.3390/electronics10030300.
[9] T. Tang, S. Yin, L. Liu, and S. Wei, "A 16K current-based 8T SRAM compute-in-memory macro with decoupled read/write and 1–5 bit column ADC," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, CA, USA, 2020, pp. 500–502.
[10] V. K. Pham and D. T. Nguyen, "Analysis of SRAM designs on TSMC 90 nm CMOS technology," *J. Sci. Technol., Da Nang Univ.*, vol. 20, no. 1, pp. 1–10, 2022, ISSN: 1859-1531.

Thanh-Trung Vu obtained his Bachelor of Engineering degree from Ho Chi Minh City University of Technology and Engineering in 2024. He is currently pursuing a master's degree in Telecomunnication Engineering at the same university in Vietnam. Since 2023, he has been working at Renesas Design Vietnam as a Hardware Engineer. His research interests are Integrated – Circuit Design, Analog Design.
- Email: 2531804@student.hcmute.edu.vn. ORCID: https://orcid.org/0009-0007-7370-0904

Tuan-Khuong Bui
- Student of Ho Chi Minh City University of Technology and Engineering, Vietnam.
- Major: Computer Engineering Technology
- Email: 18119090@student.hcmute.edu.vn. ORCID: https://orcid.org/0009-0003-0184-3245

Duc-Huy Hoang
- Student of Ho Chi Minh City University of Technology and Engineering, Vietnam.
- Major: Computer Engineering Technology.
- Email: 20119229@student.hcmute.edu.vn. ORCID: https://orcid.org/0009-0009-0826-6114

Van-Khoa Pham received his B.S. and M.S.E.E. degrees in Computer Technology and Electronics Engineering from the Ho Chi Minh City University of Technology and Engineering, Vietnam, in 2010 and 2014, respectively. In 2019, he earned his Ph.D. in Electronics Engineering from Kookmin University (KMU), Seoul, South Korea. In 2010, he joined the Integrated Circuit Design Research and Education Center (ICDREC), where he contributed to the development of the VN8-01 MCU–the first commercially designed and fabricated microcontroller in Vietnam. From May 2011 to 2021, he served as a faculty member in the Faculty of Electrical and Electronics Engineering at the Ho Chi Minh City University of Technology and Engineering (HCM-UTE). He is currently a senior lecturer in the Department of Computer and Communication Engineering. He also serves as the Head of both the Computer Engineering Technology program and the Electronics and Communications Engineering Technology program under the Faculty of International Education at HCM-UTE. His research interests include low-power VLSI design, memory design, the IoT-based applications, and AI-based solutions. He has published numerous research papers in reputable journals and conferences, including Electronics Letters, IEEE Transactions on Nanotechnology, Journal of Semiconductor Technology and Science, Micromachines, International Journal of Computing, Indonesian Journal of Electrical Engineering and Computer Science, and the IEEE International Symposium on Circuits and Systems (ISCAS).
He can be contacted at email: khoapv@hcmute.edu.vn. ORCID: https://orcid.org/0000-0002-6129-5856