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A Study on Quality of 12-Pulse Rectifier Source Feeding Three-Level T-NPC Inverter Under Switch-Open-Circuit Fault SVPWM Control

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Fault-tolerant control.

ABSTRACT

This paper studies the quality of a 12-pulse diode rectifier source feeding a three-level T-NPC inverter working under a space vector PWM control for switch-open-circuit fault, denoted as SVPWM2. Before the occurrence of the aforementioned fault, the inverter was working under conventional reduced common-mode voltage space vector PWM algorithm, denoted as SVPWM1 and providing the output voltage for a three-phase R-L load. The input and output currents of phase-shifting transformer, the input power factor of transformer, and the capacitor voltages at the DC-link are investigated. Simulation results show that the SVPWM2 method has the same characteristics as pre-fault space vector method (SVPWM1) in terms of total harmonic distortion of transformer primary and secondary currents, as well as input power factor. However, SVPWM2 has higher deviation in capacitor voltage compared to SVPWM1. Regarding to power losses, SVPWM2 has higher switching loss yet lower conduction loss than those of SVPWM1. The overall efficiency of SVPWM2 is slightly higher compared to that of SVPWM1.

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1. Introduction

Three-level (3L) T-type neutral-point-clamped (T-NPC) voltage source inverter (VSI) has several advantages compared to traditional two-level VSI (2L VSI) and 3L NPC VSI [1], [2]. The 3L T-NPC inverter is preferred to be used in high-power photovoltaic (PV) systems and low-voltage variable speed drives (VSD) [3].

Pulse-width modulation (PWM) schemes present a popular technique for controlling VSIs to made high performance and flexible output control. However, PWM techniques generate common-mode voltage (CMV). CMV is the main source of several problems in VSI-based systems, for example, causing bearing currents, which can damage the structure and lubricants of bearings part in electric machines [1], or leading to EMI noise and the deterioration of the stator insulation [1]. In order to reduce CMV for a 3L T-NPC VSI, there are a huge number of research works proposed earlier, which can be divided into two types: hardware-based solutions [4] and software-based solutions [1], [5]. Software-based solutions are preferred due to their simplicity and economic benefits. The main principle of this type of technique is to use switching vectors which CMV magnitude are zero or one-sixth of DC-link voltage [5].

The 3L T-NPC VSI has several issues regarding the reliability of operating [2], [6], [7]. For a semiconductor power switch, two typical failures can occur: switch-short-circuit (SSC) fault and switch-open-circuit (SOC) fault, respectively [8], [9]. For safety reasons, the inverter normally stops working under SSC fault [7], [10]. Another fault named SOC fault occurs due to malfunction of gate driver circuits or the lifting of bonding wire caused by thermal cycling [8], [9], [10]. This kind of fault will

lead to the deterioration of system performances, for instance, the distortion of output voltages and output currents [2] which, in turn, cause saturation in the transformer or trigger circuit protection and other effects like induced noise and vibration [10], [11].

Figure 1 shows the 3L T-NPC inverter system with 12-pulse diode-front-end rectifier. The phase-shifting transformer (PST) is fed from three-phase grid and provides two seperated outputs: one from the Y-winding and one from Δ-winding of the PST secondary windings. These output voltages feed the twelve-pulse diode rectifier, and the rectifier provides a high quality DC voltage source feeding the DC-link capacitors of the 3L T-NPC inverter. The inverter has output R-L load and is working under conventional reduced common-mode voltage (RCMV) space vector algorithm (SVPWM1).

The method for diagnosis the SOC fault on T-switch has been proposed in [10]. The average direct-axis (d-axis) current is used to determine the faulty phase, and the faulty switch is recognized by the average phase current and the neutral-point voltage variation [10].

The reliability of operation in an inverter system is essential. Therefore, it is necessary to develop an algorithm for controlling the inverter under the SOC fault conditions to prevent system interruptions. The SOC fault on a 3L T-NPC inverter can be in the T-bridge or the main bridge. If the fault is in the main bridge, the inverter's output voltage range decreases significantly [7]. By contrast, if the SOC fault is on the T-switches, the inverter can still operate with the guaranteed output voltage. The SOC fault tolerant RCMV PWM control can be divided into two types: using redundant components [6], [8], [9], and using modulation changing [10], [11], [12]. A well-known redundant type method is utilizing a fourth leg connected to the inverter [9]. This configuration offers total solution for controlling the inverter under fault condition, not only in T-bridge but also in main bridge. However, this solution has a main disadvantage of cost because it uses four additional IGBTs and three TRIACs. Besides, [9] did not consider the CMV reduction problem.

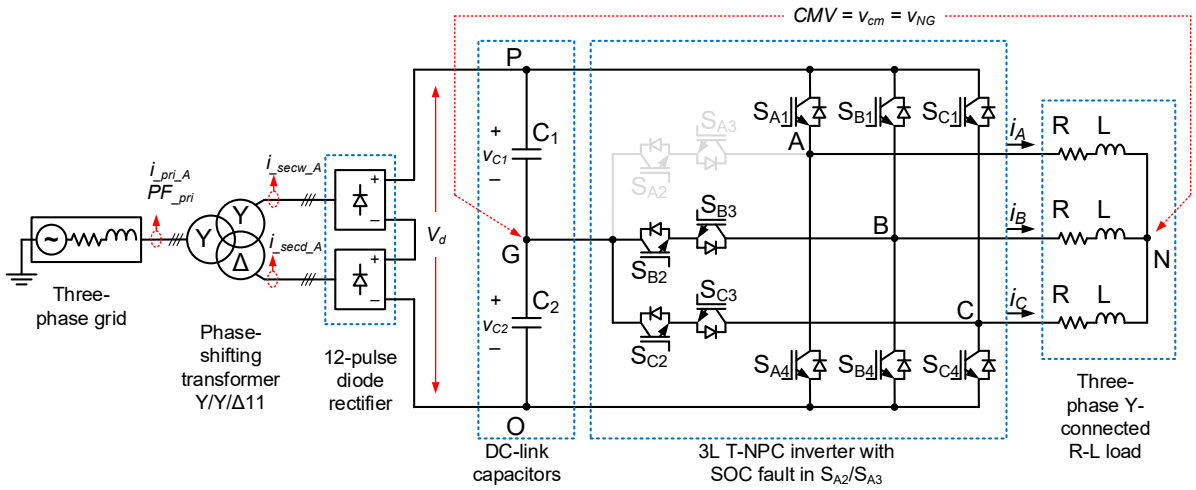

Figure 1. *A SOC fault 3L T-NPC VSI fed with 12-pulse diode rectifier for three-phase R-L load.*

In [13], a high performance SVPWM control for 3L T-NPC VSI working under the SOC fault was proposed, denoted as SVPWM2. However, study in [13] did not consider the characteristics of the PST and DC-link capacitors under the SVPWM2. For a grid-connected system, the THD of input currents is important. With different values of the modulation index of the inverter, the input currents of the 12-pulse rectifier vary in terms of both magnitudes and shapes (continuous or discontinuous mode). As a result, the input currents at the primary side of the PST also change. Besides, the fluctuation of voltage on each DC-link capacitor can exacerbate harmonics content of the inverter output. Hence, the characteristics of the input power factor (PF) and input current THD of the PST, and characteristics of DC-link capacitor voltages are neccesarily investigated in order to evaluate the effectiveness of the inverter control algorithm.

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2. Methodology

2.1. Common-mode voltage (CMV) analysis

Table 1 lists the switching states and the corresponding output voltages of 3L T-NPC VSI.

Table 1. *Switching states and output voltages of 3L T-NPC VSI, X = {A, B, C}.*

S_{X1}	S_{X2}	S_{X3}	S_{X4}	$S_X = S_{X1} + S_{X2}$	$v_{XO} = S_X(V_d/2)$	$v_{XG} = v_{XO} - V_d/2 = (S_X - 1).(V_d/2)$
0	0	1	1	0	0	$-V_d/2$
0	1	1	0	1	$V_d/2$	0
1	1	0	0	2	V_d	$V_d/2$

Refering to Figure 1, the instantaneous value of common-mode voltage, v_{cm}, can be determined by:

$$v_{cm} = v_{NG} = \left(v_{AG} + v_{BG} + v_{CG}\right)/3 \tag{1}$$

With the relationship that $v_{XG} = (S_X - 1).(V_d/2)$ with X = {A, B, C}, equation (1) becomes:

$$v_{cm} = \frac{1}{3}\left(S_A + S_B + S_C - 3\right)\frac{V_d}{2} \tag{2}$$

From (2), in order to limitation the CMV magnitude between $-V_d/6 \le v_{cm} \le +V_d/6$, the value of $(S_A+S_B+S_C)$ must be 2, 3, or 4. The space vectors satisfy this condition are shown in the space vector diagram (SVD) in Figure 2(a). The traditional RCMV space vector PWM technique, denoted as SVPWM1, can be implemented by using nearest-three-vector (NTV) and DPWM principles.

However, under SOC fault in S_{A2}/S_{A3}, the switching state of $S_A = 1$ can not be generated. Under this situation, there are only two available values of S_A, i.e. $S_A = 0$ and $S_A = 2$. The switching states of phase B and phase C are not affected by this SOC fault. Therefore, the calculation of S_B and S_C in SVPWM2 are as the same as those in SVPWM1. The number of RCMV space vectors are now reduced from 19 to 12, as shown in Figure 2(b).

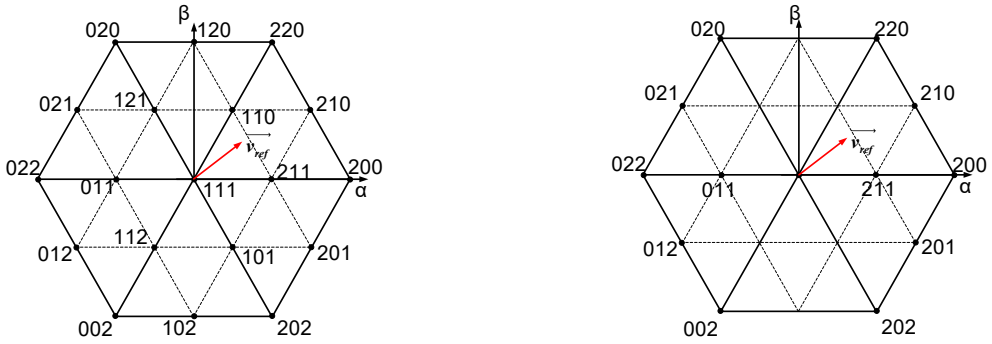


Figure 2. *RCMV space vector diagram of 3L T-NPC inverter:*
a) In normal operation (SVPWM1), b) In SOC fault occurred in one T-switch of phase A.

2.2. SOC fault control SVPWM (SVPWM2)

2.2.1. Region determination

From the SVD in Figure 2(b), in order to develope the fault-tolerant control SVPWM technique, denoted as SVPWM2, the regions on space vector diagram (SVD) are re-determined. The principles for region determination are nearest-three-vector (NTV) and discontinuous PWM (DPWM). The SVD is now divided into 24 regions, as shown in Figure 3. For example, in the first quadrant of the SVD, region 1 is determined by the NTVs {211, 210, 220} while for region 2, the set of {210, 220, 020} is selected.

For region 6, there are two available candidate sets, i.e. {210, 020, 021} and {210, 220, 021}. The set {210, 220, 021} is selected because two vectors 210 and 220 are nearer to region 6 than two vectors 020 and 021.

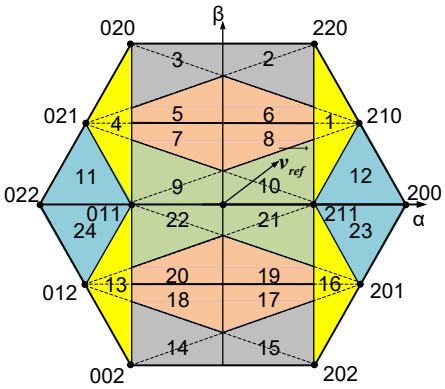


Figure 3. *Proposed regions in SVPWM2.*

2.2.2. Dwelling time calculation

Region 10 is chosen as an example for calculating dwelling time. The formula to synthesize $\overrightarrow{v_{ref}}$ is as follows:

$$\begin{cases} \overrightarrow{v_{ref}} = d_1\vec{v}_1 + d_2\vec{v}_2 + d_3\vec{v}_3 \\ d_1 + d_2 + d_3 = 1 \end{cases} \tag{3}$$

where d_1, d_2, and d_3 are the dwelling factors corresponding to $\vec{v}_1$, $\vec{v}_2$, and $\vec{v}_3$, respectively, and $0 \le d_1, d_2, d_3 \le 1$. The values of each vector are $\vec{v}_1 = \left(1/2 + j\sqrt{3}/6\right)$, $\vec{v}_2 = 1/3$ and $\vec{v}_3 = -1/3$, respectively. Solving (3) in α-β coordinates leading to the following results:

$$d_1 = d_{210} = 2A, d_2 = d_{211} = \left(-5A + B + 1\right)/2, d_3 = d_{011} = \left(A - B + 1\right)/2 \tag{4}$$

in which $A = m.\sin\theta$ and $B = m\sqrt{3}.\cos\theta$. The value $m = \sqrt{3}V_{ref}/V_d$ is the modulation index. For this study, the maximum value of m is 1.

2.2.3. Space vector implementation

Table 2 lists the nearest-three vector (NTV) selection, the duty factors, and pulse patterns for the proposed algorithm for all 24 regions.

Table 2. *Space vector implementation of SVPWM2.*

Region	NTV selection	Duty factors	Pulse pattern
1	211, 210, 220	$d_{211} = -A - B + 2, d_{210} = 2B - 2, d_{220} = A - B + 1$	211-210-220-210-211
2	210, 220, 020	$d_{210} = -2A + 2, d_{220} = \left(5A + B - 4\right)/2, d_{020} = \left(-A - B + 2\right)/2$	210-220-020-220-210
3	021, 020, 220	$d_{021} = -2A + 2, d_{020} = \left(5A - B - 4\right)/2, d_{220} = \left(-A + B + 2\right)/2$	021-020-220-020-021
4	011, 021, 020	$d_{011} = -A + B + 2, d_{021} = -2B - 2, d_{020} = A + B + 1$	011-021-020-021-011
5	021, 020, 210	$d_{021} = \left(-5A - B + 4\right)/3, d_{020} = 2A - 1, d_{210} = \left(-A + B + 2\right)/3$	021-020-210-020-021
6	210, 220, 021	$d_{210} = \left(-5A + B + 4\right)/3, d_{220} = 2A - 1, d_{021} = \left(-A - B + 2\right)/3$	210-220-021-220-210
7	021, 011, 210	$d_{021} = \left(5A - B - 1\right)/3, d_{011} = -2A + 1, d_{210} = \left(A + B + 1\right)/3$	021-011-210-011-021

8	210, 211, 021	$d_{210}=(5A+B-1)/3, d_{211}=-2A+1, d_{021}=(A-B+1)/3$	210-211-021-211-210
9	021, 011, 211	$d_{021}=2A, d_{011}=(-5A-B+1)/2, d_{211}=(A+B+1)/2$	021-011-211-011-021
10	210, 211, 011	$d_{210}=2A, d_{211}=(-5A+B+1)/2, d_{011}=(A-B+1)/2$	210-211-011-211-210
11	011, 021, 022	$d_{011}=-A+B+2, d_{021}=2A, d_{022}=-A-B-1$	011-021-022-021-011
12	211, 210, 200	$d_{211}=-A-B+2, d_{210}=2A, d_{200}=-A+B-1$	211-210-200-210-211
13	011, 012, 002	$d_{011}=A+B+2, d_{012}=-2B-2, d_{002}=-A+B+1$	011-012-002-012-011
14	012, 002, 202	$d_{012}=2A+2, d_{002}=(-5A-B-4)/2, d_{202}=(A+B+2)/2$	012-002-202-002-012
15	201, 202, 002	$d_{201}=2A+2, d_{202}=(-5A+B-4)/2, d_{002}=(A-B+2)/2$	201-202-002-202-201
16	211, 201, 202	$d_{211}=A-B+2, d_{201}=2B-2, d_{202}=-A-B+1$	211-201-202-201-211
17	201, 202, 012	$d_{201}=(5A+B+4)/3, d_{202}=-2A-1, d_{012}=(A-B+2)/3$	201-202-012-202-201
18	012, 002, 201	$d_{012}=(5A-B+4)/3, d_{002}=-2A-1, d_{201}=(A+B+2)/3$	012-002-201-002-012
19	201, 211, 012	$d_{201}=(-5A+B-1)/3, d_{211}=2A+1, d_{012}=(-A-B+1)/3$	201-211-012-211-201
20	012, 011, 201	$d_{012}=(-5A-B-1)/3, d_{011}=2A+1, d_{201}=(-A+B+1)/3$	012-011-201-011-012
21	201, 211, 011	$d_{201}=-2A, d_{211}=(5A+B+1)/2, d_{011}=(-A-B+1)/2$	201-211-011-211-201
22	012, 011, 211	$d_{012}=-2A, d_{011}=(5A-B+1)/2, d_{211}=(-A+B+1)/2$	012-011-211-011-012
23	211, 201, 200	$d_{211}=A-B+2, d_{201}=-2A, d_{200}=A+B-1$	211-201-200-201-211
24	011, 012, 022	$d_{011}=A+B+2, d_{012}=-2A, d_{022}=A-B-1$	011-012-022-012-011

The block diagram for implementation SVPWM2 is shown in Figure 4.

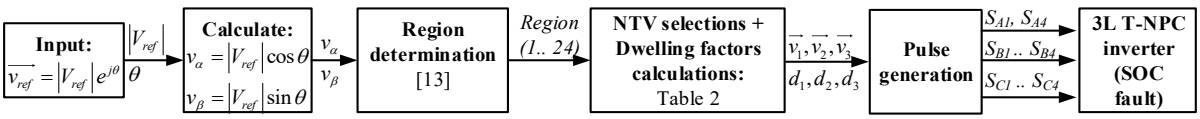


Figure 4. *Control structure of the T-NPC inverter system.*

3. Simulation Results

A MATLAB/Simulink model was built to simulate the system in Figure 1. Simulation parameters are listed in Table 3.

Table 3. *Simulation parameters.*

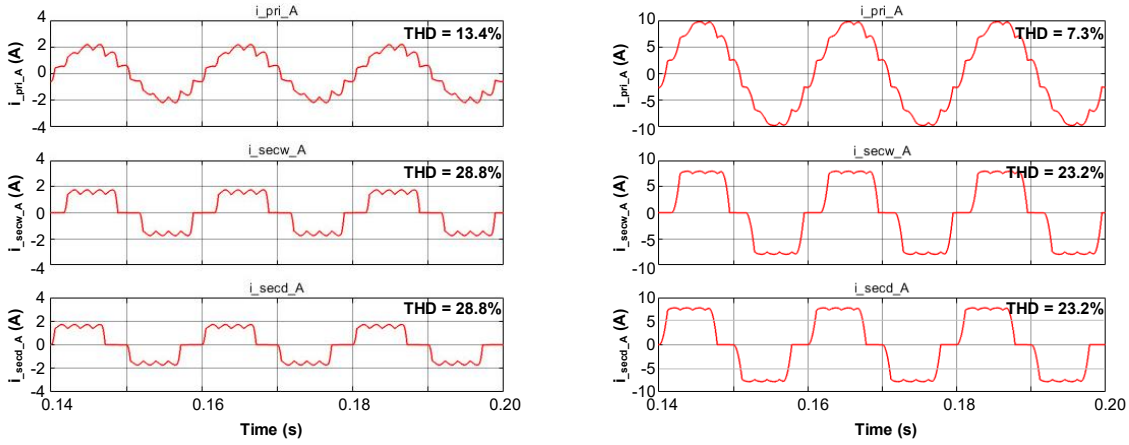
Parameter	Notation	Value	Unit
Grid voltage (line voltage)	V_g	400	V
Transformer rated apparent power	S_B	10000	VA
Transformer secondary wye-winding voltage	V_2	230	V
Transformer secondary delta-winding voltage	V_3	230	V
Rated DC-link voltage	V_d	600	V
DC-link capacitances	C_1, C_2	2000×10^{-6}	F
Fundamental output frequency	f	50	Hz

Switching frequency	f_{sw}	5000	Hz
Load resistance	R	16	Ω
Load inductance	L	0.050	H

3.1. Simulation results for PST

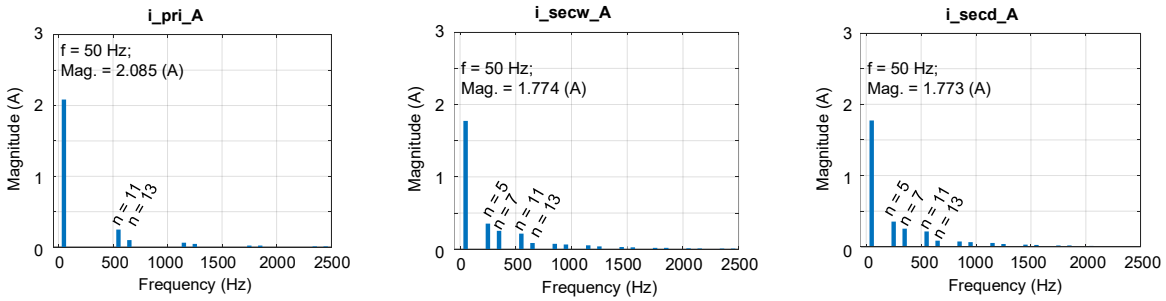
Figure 5 shows the waveforms of primary current ($i_{\_pri\_A}$), secondary wye-winding current ($i_{\_secw\_A}$), and secondary delta-winding current ($i_{\_secd\_A}$) of the PST corresponding to m = 0.4 and m = 0.9. The spectra of these current are shown in Figure 6 (m = 0.4) and in Figure 7 (m = 0.9), respectively.

The spectra of $i_{\_pri\_A}$ in Figure 6(a) and Figure 7(a) do not have 5th and 7th harmonic components, and the 17th and 19th components are inconsiderable. By contrast, the spectra of $i_{\_secw\_A}$ and $i_{\_secd\_A}$ have these odd harmonics components, i.e. 5th, 7th, 11th and 13th harmonic order.



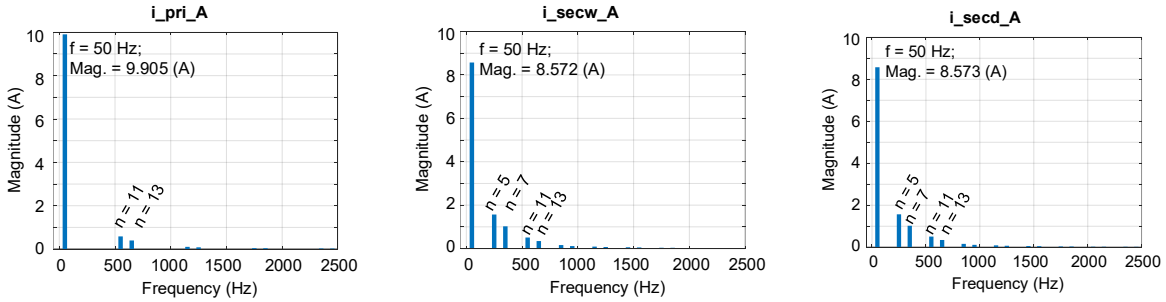
(a) *(b)*

Figure 5. *Waveforms of PST currents: a) m = 0.4, and b) m = 0.9 (f_{maxFFT} = 2.5 kHz). From top to bottom: $i_{\_pri\_A}$, $i_{\_secw\_A}$, and $i_{\_secd\_A}$.*



(a) *(b)* *(c)*

Figure 6. *Spectra of PST currents with m = 0.4: a) $i_{\_pri\_A}$, (b) $i_{\_secw\_A}$, and c) $i_{\_secd\_A}$ (f_{maxFFT} = 2.5 kHz).*



(a) *(b)* *(c)*

Figure 7. *Spectra of PST currents with m = 0.9: a) $i_{\_pri\_A}$, (b) $i_{\_secw\_A}$, and c) $i_{\_secd\_A}$ (f_{maxFFT} = 2.5 kHz).*

The THD characteristics of i_{pri_A} is shown in Figure 8(a), and primary side power factor (PF_{pri}) is shown in Figure 8(b). For comparison purpose, characteristics of SVPWM2 are presented along with those of SVPWM1, which is the SVPWM method for controlling the inverter before the occurrence of SOC fault. From Figure 8, SVPWM2 has the same characteristics compared to SVPWM1. With m > 0.6, THD(i_{pri_A}) is less than 10%. The transformer has high input power factors (PF_{pri} > 0.97) in the whole range of modulation index.

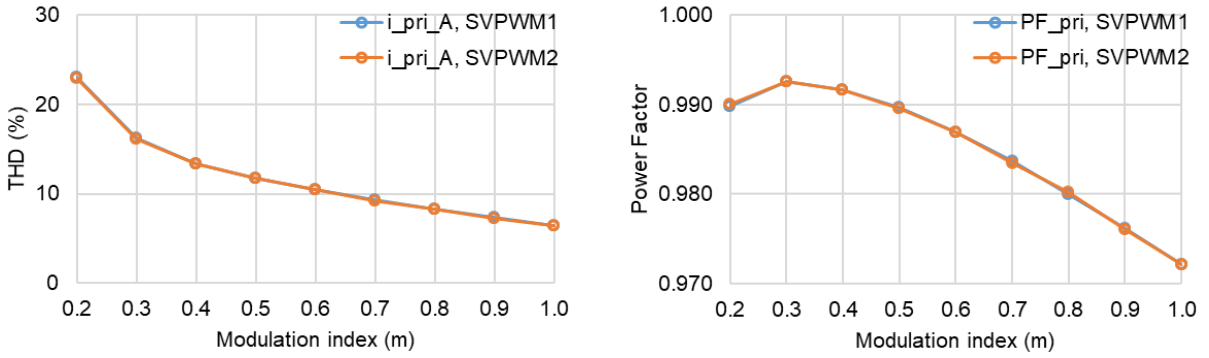


Figure 8. *PST primary side characteristics versus modulation index (m): a) THD of i_{pri_A} (f_{maxFFT} = 2.5 kHz), and b) Input PF (PF_{pri}).*

Regarding to THD characteristics of secondary currents (i_{secw_A} and i_{secd_A}), from Figure 9 it is seen that the SVPWM2 also has the same behavior as SVPWM1 in the whole range of m. THD characteristics of i_{secw_A} and i_{secd_A} are identical.

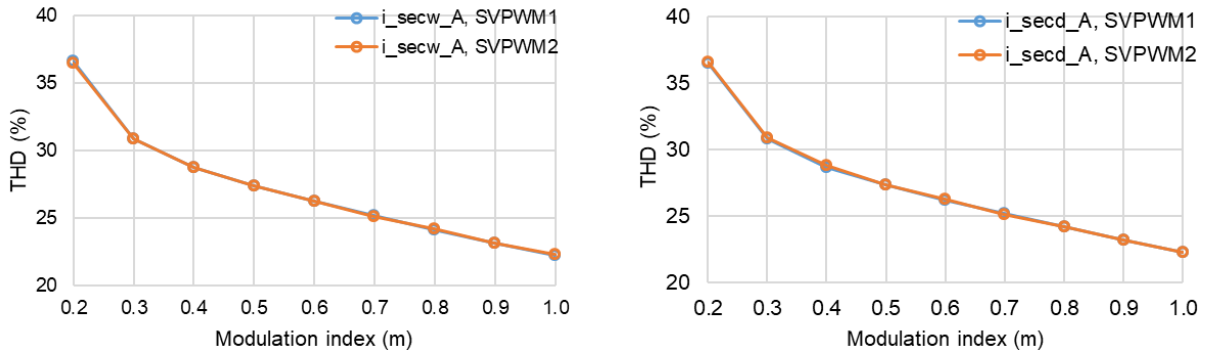
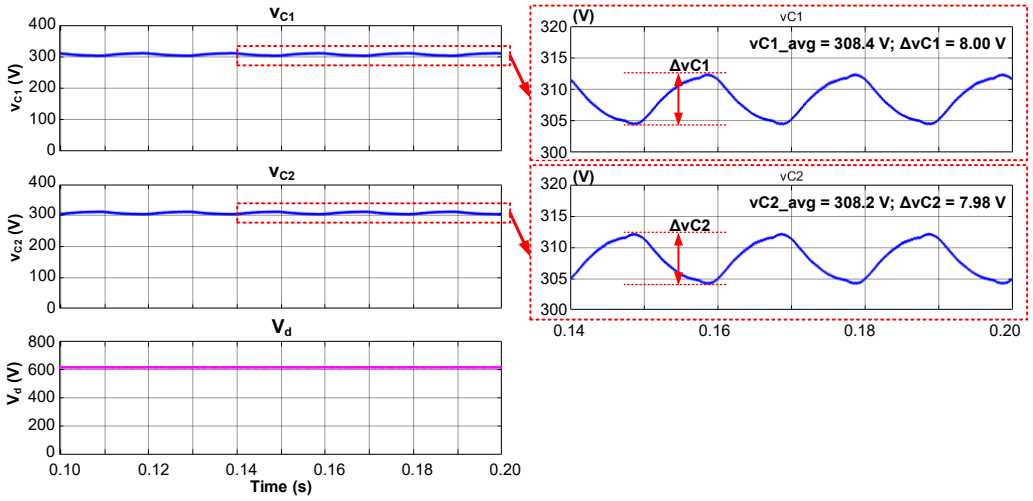


Figure 9. *PST secondary current THD characteristics versus modulation index (m): a) i_{secw_A}, and b) i_{secd_A} (f_{maxFFT} = 2.5 kHz).*

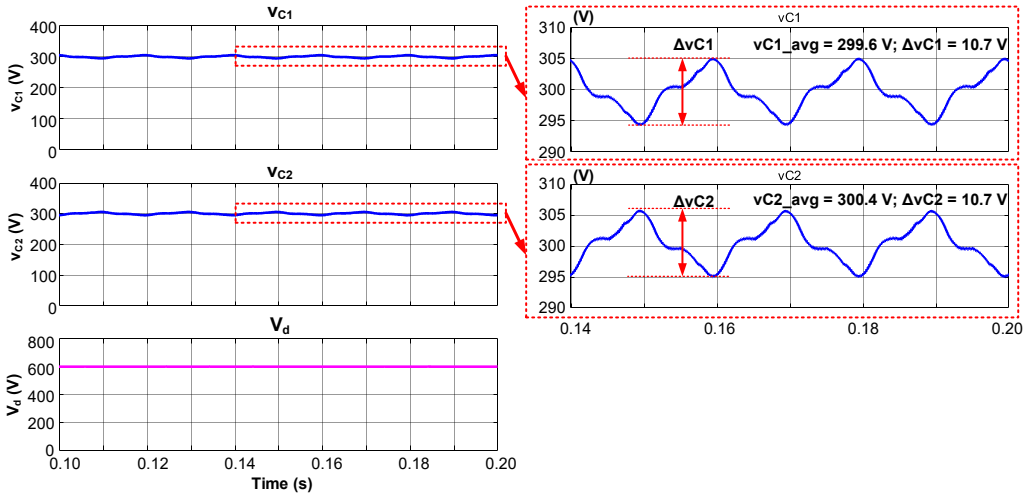
3.2. Simulation results for DC-link capacitors

The waveforms of capacitor voltages and DC-link voltage in SVPWM2 are shown in Figure 10. Each capacitor shares a half of DC-link voltage. At low modulation index (m = 0.4), the average voltage on each capacitor is slightly higher than rated value: v_{C1_avg} = 308.4 V and v_{C2_avg} = 308.2 V, and the voltage ripple on each capacitor is about 8 V. For high value of m (m = 0.9), the voltage ripple increase to 10.7 V. At m = 0.9, each capacitor has the voltage as rated value, i.e. 300 V.

The characteristics of capacitor voltage ripple are shown in Figure 11. Overall, all ripples are lower than 4%. The SVPWM2 has higher ripple compared to SVPWM1 which is about 2 times for m > 0.7. For example, at m = 0.9, Δv_{C1} and Δv_{C2} in SVPWM2 are 3.6% while those in SVPWM1 are 1.7%.



(a)



(b)

Figure 10. *DC-link voltage waveforms for SVPWM2:*
a) m = 0.4, b) m = 0.9. From top to bottom: C1 voltage (v_{C1}), C2 voltage (v_{C2}), and total DC-link voltage (V_d).

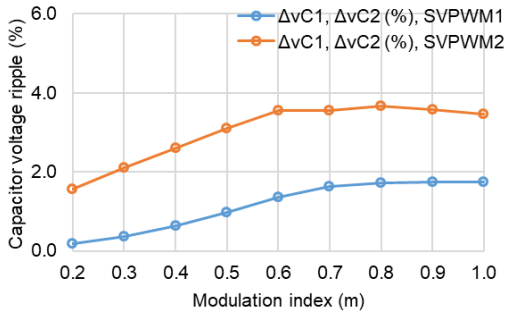
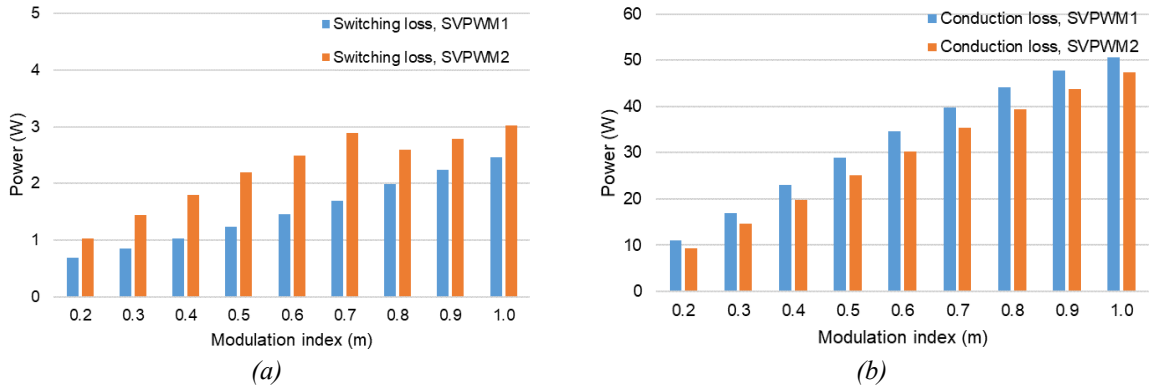


Figure 11. *Voltage ripple characteristics of DC-link capacitors (Δv_{C1}, Δv_{C2} normalized to rated V_{C1} and V_{C2}) versus modulation index (m).*

3.3. Simulation results for loss evaluation

A PLECS simulation model was built in order to calculate power losses. Figure 12 shows the switching loss and conduction loss of SVPWM2 compared to SVPWM1. The efficiency characteristics are presented in Figure 13. From Figure 12(a), SVPWM2 has higher switching loss than SVPWM1, especially at low modulation index (m <0.7). However, the conduction loss of SVPWM2 is lower than that of SVPWM1, as shown in Figure 12(b). Overall, the efficiency of SVPWM2 is slightly higher than SVPWM1, as shown in Figure 13.



(a) *(b)*

Figure 12. *Power losses of SVPWM2 and SVPWM1 versus modulation index: a) Switching loss, and b) Conduction loss.*

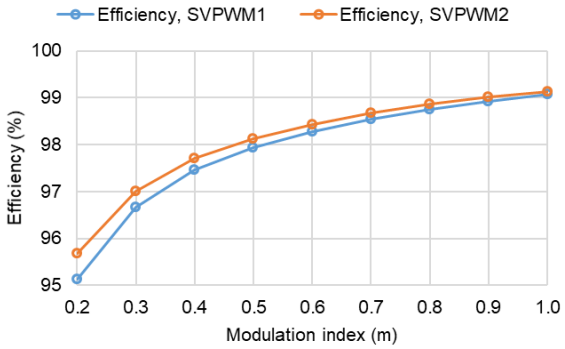


Figure 13. *Efficiency of SVPWM2 and SVPWM1 versus modulation index.*

4. Conclusion

This paper presents the quality of a 12-pulse rectifier feeding a 3L T-NPC VSI working under SVPWM control for SOC fault. The transformer currents and capacitor voltages are measured and analyzed in different values of the inverter modulation indices. Simulation results show that SVPWM2 has the same characteristics as SVPWM1 in terms of transformer input and output currents, and transformer input power factor for the whole range of modulation indices. However, SVPWM2 has higher capacitor voltage ripples compared to SVPWM1. Compared to previously proposed methods for controlling the T-NPC inverter under SOC fault, SVPWM2 is more economic due to the fact that this method does not required any additional hardware. In addition, based on the re-design of SVPWM control, the output voltage of the inverter could be as high as pre-fault SVPWM1.

The potential avenues for future research are as follows:

1) Implementing SVPWM2 using carrier-based PWM (CBPWM) principle. This type of PWM method is simple in calculation and implementation compared to SVPWM.

2) Developing a RCMV model predictive control (MPC) algorithm for controlling the inverter under SOC fault. MPC is a popular method used recent years for power electronics converters. Due to the number of RCMV vectors is reduced from 19 (in SVPWM1) to 12 (in SOC fault), the computation burden of this method can also be reduced.

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Conflict of interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

Table of abbreviations

Abbreviations	Definition
CMV	Common-Mode Voltage
DPWM	Discontinuous Pulse-Width Modulation
ESPWM	Eight-Switch Pulse-Width Modulation
ESTPI	Eight-Switch Three-Phase Inverter
NPC	Neutral-Point-Clamped
NTV	Nearest-Three-Vector
PST	Phase-Shifting Transformer
PWM	Pulse-Width Modulation
RCMV	Reduced Common-Mode Voltage
SOC	Switch-Open-Circuit
SSC	Switch-Short-Circuit
SVD	Space Vector Diagram
SVPWM	Space Vector Pulse-Width Modulation
THD	Total Harmonic Distortion
T-NPC	T-Type Neutral-Point-Clamped
VSD	Variable Speed Drives
VSI	Voltage Source Inverter

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