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Design, Simulate, and Layout for a Static Random-Access Memory (SRAM) Using a 6T Memory Cell and a Latch-Based Sense Amplifier

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ABSTRACT

This study focuses on the implementation and assessment of a 64-bit SRAM (Static Random-Access Memory) design utilizing 6T memory cells. The objective of this SRAM design, as presented in this study, is to explore its structure, functionality, and key attributes. To achieve this, the Cadence Virtuoso tool is employed for both design implementation and evaluation, utilizing the CMOS technology library. The design incorporates 6T memory arrays, which are commonly used in modern SRAM designs, along with additional peripheral components for efficient array management. The memory circuit will be constructed using the Virtuoso Schematic Editor, and its physical layout will be created using the Virtuoso Layout Suite XL. The read and write operations are validated through timing diagrams for various scenarios. Furthermore, the stability of the 6T memory cells is ensured by conducting an SNM (Static Noise Margin) analysis. From a layout perspective, each component undergoes thorough verification for Design Rule Checking (DRC) and Layout vs. Schematic (LVS) using the Assura tool.

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1. Introduction

As electronic devices have reached a size limit, System on Chips (SoCs) offer a new proposition to the competitive market with their advantages such as enhanced performance, reduced power consumption, and smaller semiconductor die area. SoCs encounter a performance bottleneck due to the disparate operating speeds of the main memory and the CPU. One strategy to mitigate this bottleneck is the use of cache memory, composed of Static Random-Access Memory (SRAM) cells. Moreover, SRAM has the highest integration densities, consuming the majority of a typical SoC's transistors [1]. Therefore, the design of a low latency, low power SRAM memory is crucial in the development of SoCs and computing systems in general.

In a prior investigation [2], researchers presented a design for a 32KB synchronous SRAM module utilizing a 6-transistor (6T) memory cell structure within a 90nm Complementary Metal-Oxide Semiconductor (CMOS) UMC technology. The SRAM design incorporates essential features such as row and column redundancy, pre-decoder, column multiplexer, and self-timing circuitry. Comprehensive simulations were conducted to evaluate read/write performance, cycle time, and power consumption across various process corners. However, the study lacks detailed circuitry information for each specific instance and their corresponding operations.

In the publication [3], three distinct design approaches are proposed to achieve high-performance, low-power synchronous single-port 1024x32 SRAM using 28nm technology. These methods encompass folding with a 4-to-1 column multiplexer, pre-decoding, and a tracking technique. Rigorous simulations are conducted to assess power consumption, leakage current, and memory cycle time. Additionally, the study investigates the read/write behavior of the memory under different process, voltage, and

temperature (PVT) variations. Similar to the preceding study [2], this paper primarily focuses on analyzing the operational aspects of the proposed SRAM design but does not provide a detailed view of the specific circuit instances. Furthermore, while the setup and hold time for data are analyzed, the corresponding setup and hold time for addresses remain unaddressed.

In the research endeavor [4], the author delves into the design and analysis of a 6T, 128x128 low-voltage SRAM, leveraging the self-timed dummy replica technique within TSMC's 180nm technology. The circuitry details for all instances of SRAM are meticulously presented. The study includes simulations covering read/write operations, self-timed functionality, and sense amplifier behavior. Additionally, the access time of the proposed memory is thoroughly examined across scenarios involving both high and low data cases.

Furthermore, the study [5] introduces the design and implementation of an 8K-bit, low-power SRAM utilizing 180nm technology. The research emphasizes low-power design techniques, including sub-array memory, multi-stage decoding, and dynamic NOR decoding. Key aspects such as the Static Noise Margin (SNM) of the memory cell, peripheral operation, and read/write performance are rigorously analyzed through simulations and waveform studies.

The size of the SRAM cell is being reduced using scaling over the past three decades [5]. The scaling techniques also have their drawbacks such as higher leakage and bigger delay, which then cause more power consumption and slower operation. Recognizing the importance of designing an appropriate SRAM, this work concentrates on constructing a low power, high speed 64 bits 6T SRAM based on TSMC technology. The layout of the designed SRAM will be designed and presented using Virtuoso Cadence. Additionally, simulations will be conducted to demonstrate the performance of the memory in terms of power dissipation, Signal-to-Noise Margin (SNM), and Read/Write delay.

2. Materials and Methods

2.1. SRAM Read/Write Operation

SRAM retains data in the form of binary bits, with each bit stored in a unit referred to as a "cell". Traditional SRAM cells comprise six transistors that form cross-coupled CMOS inverters and a pair of pass gates M5 – M6, as depicted in Figure 1a. These two pass gates can be toggled by the wordline (WL) signal. When WL = '1', the cell is selected for either read or write operation. The input/output of the two inverters is designed to connect in a positive feedback configuration, creating a flip-flop design to store binary data at positions Q and Q_bar. The stored data values are delivered to the bitline (BL) and bitline bar (BLB) lines through the switching on/off of the corresponding transistors M5 and M6.

Figure 1b presents the CMOS level schematic of a 6T SRAM cell with transistors M1 – M6. M1 and M3 serve as pull-down transistors, while M2 and M4 function as pull-up transistors of the cross-coupled inverters. When the WL is selected, the corresponding bitlines (BLs) are connected to Q and Q_bar. The Static Random Access Memory (SRAM) operates in three basic modes: write, read, and hold data. In the data hold mode, the WL signal line is not activated, leading to transistors M5 and M6 ceasing conduction, and the BT and BB signal lines being completely isolated from the data storage cell [6]. Consequently, the SRAM cell will retain the state of the data that was previously written. In the case of a read operation, the wordline will be triggered, and data stored in Q and Q_bar nodes will be transferred to the corresponding bitlines. Conversely, during a write operation, the bitlines will drive Q or Q_bar down to the VSS level to write the desired data to the bitcell.

(a) (b)

Figure 1. *6T SRAM Cell Schematic: (a) Logic Gate Level [7]; (b) CMOS Level [8].*

During the read operation, the values stored in Q and Q_bar are transferred onto the BLs. Let's assume that the bit stored in this cell is '0'. Prior to the activation of the WL, the BLs are pre-charged to VDD by the pre-charge circuit. The WL is then triggered, which turns on the pass gates M5 – M6. Given that Q is '0', a voltage difference arises between BL and Q. In this scenario, the active transistors are M2 and M3 because Q = '0' and Q_bar = '1'. While BL_bar remains at a high level, BL discharges through M3. This process results in a voltage difference between the BLs. The sense amplifier circuit is tasked with detecting this difference and amplifying it. In the converse case where Q stores '1', the process is identical, but the discharge process occurs on BL_bar.

In order to write data to a cell, one of the bitlines is utilized to pull the cell to VSS. Let's assume that in this scenario, '1' is written into a cell that initially contains '0'. Similar to the read operation, the bitlines are pre-charged to VDD prior to triggering the wordline. With Q = '0' and Q_bar = '1' initially, M2 and M3 are activated, connecting Q_bar to VDD and Q to VSS. New data, in this case, bit '1', is loaded in courtesy of the data latch and write driver. The value of this new data determines which bitline will be tied to VSS. To write bit '1' into the cell, BL_bar must be tied to the ground. Once the WL is triggered and the cell is selected, the BLs are connected to Q and Q_bar. BL_bar pulls Q_bar down to VSS and switches M4 on, connecting Q to VDD. After the wordline is triggered, BL_bar pulls Q_bar to VSS and flips the Q value from '0' to '1'. The slight increase in Q voltage at the beginning is due to BL discharging through M3. However, the driver pulling BL_bar down is significantly stronger, ensuring that this discharging process does not impact the operation.

2.2. Power Consumption and Signal Noise Margin (SNM)

SRAM memory contains billions of transistors which switches their states frequently. The power consumption in SRAM design mostly comes from the switching of transistors in read/write operation and the leakage current in its inactive state. There are many methods had been proposed to decrease the power dissipation of SRAM memory such as power gating, self-timing circuit, dual-rail memory, etc., in which, additional circuits must be inserted to the memory. These circuits have bad impact on the memory performance and its area. Hence, the power consumption optimization in an SRAM design should be significantly studied. To determine the power dissipation of a circuit, the power should be observed over a period of time. Because the power consumption at different point of time is significantly different depending on the operation at that point. The average power consumption over a period of time is considered the power dissipation of a circuit. Average power over period time T can be calculated by the given equation (1):

$$P(t) = \frac{1}{T}\int_0^T P(t)dt \tag{1}$$

The total power consumption of a circuit comes from the power consumed in its active state and the power consumed in its idle state as given in the equation (2). Active power is the power consumed while the chip is doing useful work. As mentioned above, the dynamic power of an SRAM memory is mostly contributed by the switching of transistors in read/write operations. Meanwhile, the power consumed in idle state is the unwanted leakage which comes from the leak currents through inactive transistors. In nanometer processes with low threshold voltages and thin gate oxides, leakage can account for as much as a third of total active power [9].

$$Ptotal = Pdynamic + Pstatic \tag{2}$$

3. SRAM Memory Implementation

3.1. System design

Figure 2 illustrates the block diagram of an entire 8x8 SRAM memory. The design is partitioned into five principal blocks such as Control Block, Address Decoder Block, Memory Cell Array, Periphery Block, and IO Block.

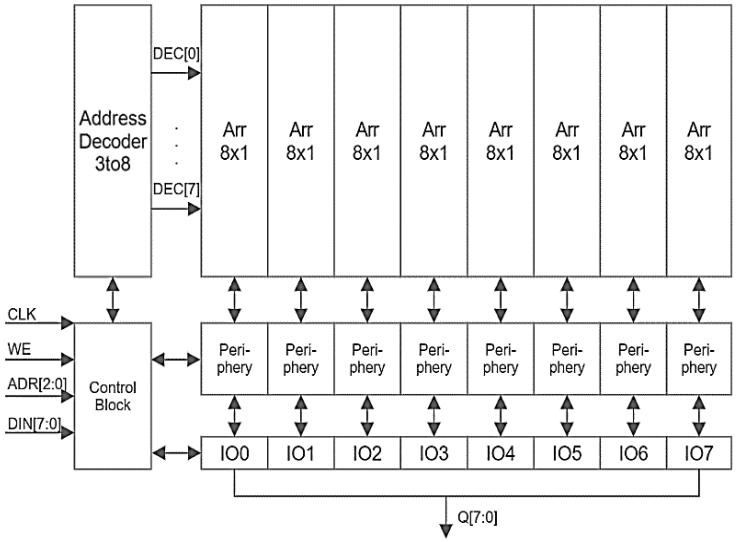


Figure 2. *8 by 8 SRAM Block Diagram.*

The Control Block encompasses circuitry for generating internal clock pulses, which are utilized for managing the racing of signals. Additionally, this block houses latch circuitry for securing input signals. It also includes circuits that generate peripheral control signals for read/write operations. The Address Decoder Block is a 3 to 8 decoder that uses an address as input. The output of this block is an 8-bit signal, which is employed to select the desired wordline for read or write operations.

The Array Block comprises 64 SRAM memory bitcells, which are arranged into 8 rows and 8 columns, with a specific address for each row. Bitcells in the same column are amalgamated to form an 8x1 array. The Periphery Block consists of Pre-charge, Sense Amplifier, Write Driver, and Read/Write Pass Gating circuit. This block is responsible for the read and write functions of the memory. The IO Block manages the data input and data output of the memory using the Data Input Latch and Data Out Latch circuit situated within the block.

In an SRAM design, there are two primary operations: reading data contained in selected bitcells and writing data to selected bitcells. The selection of bitcells is facilitated by the address decoder, while the read/write selection is controlled by the Write Enable input signal (WE). For the read operation, the control block generates Pre-charge and Sense Amplifier control signals to read data from selected bitcells. The output data is latched out and can be accessed through the IO block. For the write operation, the control block generates the control signals for Precharge and Write Driver to write the data input, which is latched in by the Data Input Latch in the IO block, into selected bitcells.

An 8x1 array is composed of eight 6T bitcells that share identical bitlines. These shared bitlines are linked to the periphery of the column. The selection of a bitcell is achieved by activating its wordlines. The WL bus is a shared resource among the arrays. Upon the selection of a WL, the bitcells from these rows are chosen, enabling the execution of read/write operations. The assembly of the array block requires eight 8x1 arrays.

The control circuit is in charge of generating periphery control signals. Figure 3 describes the schematic diagram of a Control Circuit.

Table 1. *Control Circuit Truth Table.*

CLK	WE	PRCHB	SAPR	SAE	WPASS	RPASS
0	0	0	0	0	0	1
0	1	0	0	0	0	1
1	0	1	1	1	0	0
1	1	1	0	0	1	1

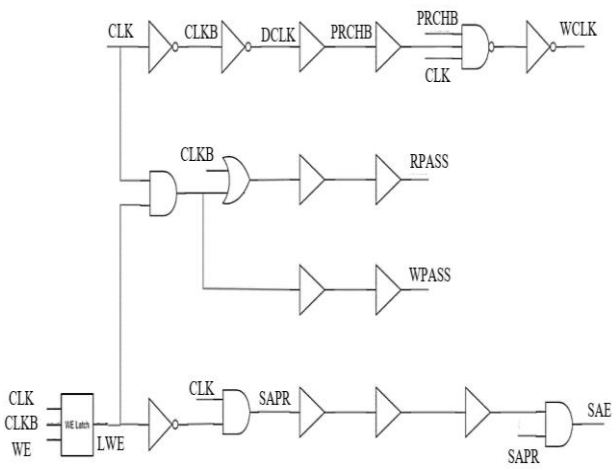


Figure 3. *Schematic Diagram of Control Circuit.*

The inputs of the circuit are CLOCK signal (CLK) and WE. The outputs of the circuit are:

- PRCHB: This signal is used for turn on Pre-charge.
- DCLK: Clock signal used for latching new data input.
- WCLK: Clock signal used for triggering address decoder to generate WL signal.
- SAPR: This signal is used for turn on Sense Amplifier Pre-charge.
- SAE: This signal is used for enable Sense Amplifier, reading the data out.
- WPASS/RPASS: These signals are used for selecting read or write operation.

The design of the control circuit is predicated on the desired states of the signal during read operations, write operations, and during the low clock cycle when the memory is reset for a new cycle. The truth table delineating these states is provided in Table 1.

In the context of selecting a specific row for read or write operations, it is essential to provide the address corresponding to that row. To achieve this, an address decoder is utilized, which translates 3-bit address inputs (ADR<0:2>) into 8-bit Wordline selection signals. These output signals from the decoder are subsequently gated with the WCLK (Wordline Clock) signal, as depicted in Figure 4. The purpose of the WCLK signal is to enhance the slew rate of the Wordline (WL). Without the presence of the WCLK signal, the decoder's address decoding process could potentially lead to suboptimal slew characteristics for the WL.

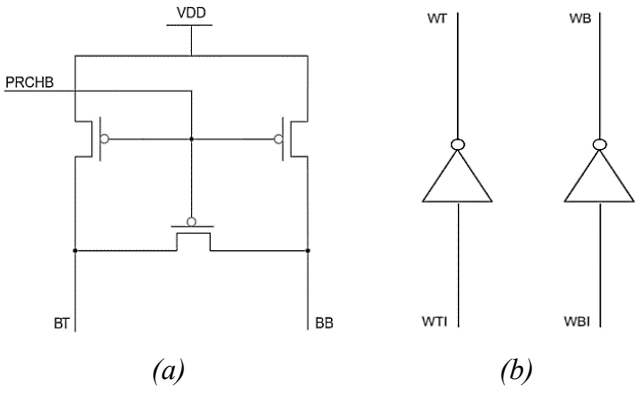


Figure 5. *Schematic Diagram of: (a) Pre-charge; (b) Write Driver.*

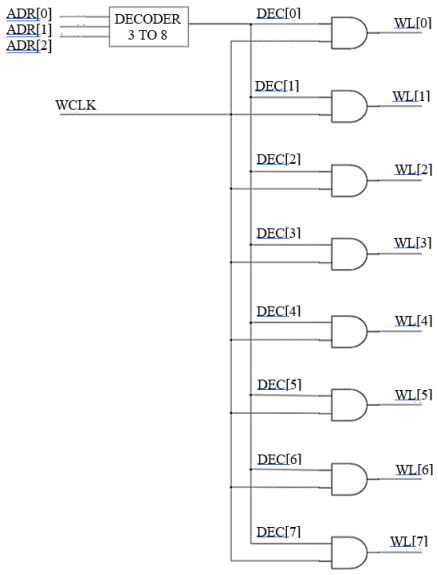


Figure 4. *Schematic Diagram of Address Decoder with Gating WCLK.*

The peripheral block of the memory module comprises several essential components: a pre-charge circuit, a sense amplifier, a write driver, and a read/write pass circuit. The pre-charge circuit serves the purpose of pre-charging the bitlines to the supply voltage (VDD) before read or write operations. During read operations, pre-charging the bitlines ensures that the voltage difference between them, after sensing

the bitcells, can be accurately compared. In write operations, pre-charging the bitlines ensures that after pulling one bitline down, the other bitline remains at the VDD level. Figure 5a provides the schematic representation of the pre-charge circuit. The write driver circuit is relatively straightforward, consisting of two large inverters, as depicted in Figure 5b. These oversized inverters are intentionally designed to be robust enough to effectively pull down the bitlines. After latching the new data for a write operation, the inverted values of the bitlines pass through these driving inverters, resulting in the pulling down of one write bitline. By selectively pulling down one write bitline while maintaining the other at the VDD level, data can be successfully written into the bitcell.

For sensing such a small voltage difference between the bitlines, a sense amplifier is necessary for reading bitcell's value. A differential sense amplifier as shown in Figure 6a amplifies the voltage difference between two input signals. It multiplies the difference between these input signals, making it useful for various applications, including noise reduction and precision signal detection. The key feature of differential amplifiers is their ability to reject common-mode noise while amplifying the differential signal [10]. Latch-based sense amplifiers as shown in Figure 6b are commonly used in memory circuits. They rapidly sense and amplify small voltage changes on bitlines during read operations. Latch-based sense amplifiers [11] operate in current mode, responding to the differential current rather than the voltage between inputs. Compared to differential sense amplifier, Latch-based sense amplifiers offer rapid response times. Besides, Latch-based sense amplifiers significantly reduce bit-line voltage swings. This reduction minimizes energy consumption and improves overall efficiency. This design also provides adequate noise margins. In summary, differential sense amplifiers excel in noise rejection and precision, while latch-based sense amplifiers focus on speed, reduced voltage swing, and efficient noise margins.

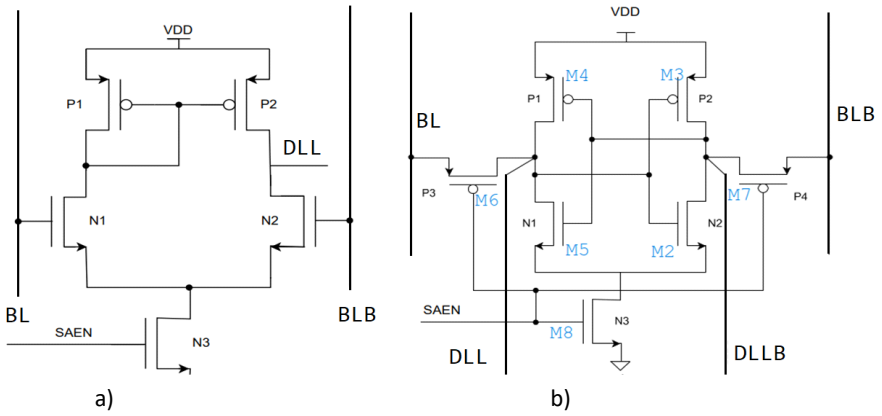


Figure 6. *Schematic Diagram of a) Differential sense amplifier b) Latch-based sense amplifiers.*

Figure 7a illustrates the operation of the DSA circuit during the reading of ‘0’ and ‘1’ data from the memory cell. The stored values Q and Q_b of the SRAM memory cell determine the functional accuracy of the sense amplifier circuit during read operations. Figure 7a clearly shows the process of reading a ‘0’ from the memory cell when both the WL and SAEN signals are simultaneously activated (high level), and the DSA circuit output is DLL. This logic value corresponds to the value read by BL from the SRAM memory cell. The process of reading a ‘1’ by the DSA sense amplifier is depicted in Figure 7a when the DLL value, after an access period, matches the logic level of BL. Figure 7b demonstrates the operational function of the LSA design in two scenarios: reading 0 and reading 1 from the memory cell. When the WL signal enables the bit cell for reading, the BL/BLB signals gradually read data from the bit cell. Subsequently, the SAEN signal is activated (set to 1), enabling the LSA circuit, which causes both DLL and DLLB output signals to be immediately pulled down by a certain voltage. Notably, these two signals change states together until DLL surpasses the trip point first, causing the LSA circuit to flip and the DLLB output signal to switch to ‘1’. Ultimately, DLL will reflect the ‘0’ data value, matching the ‘0’ stored in the bit cell at point Q. The process of reading a ‘1’ from the memory to the DLL and DLLB outputs is also shown in Figure 7b. When the WL signal is activated, DLL will sense the data on the BL signal and accurately read the ‘1’ value stored in Q. For DLLB, the signal will show

the opposite, where the '0' value read by DLLB corresponds to the data read by BLB from Q_b in the SRAM memory cell.

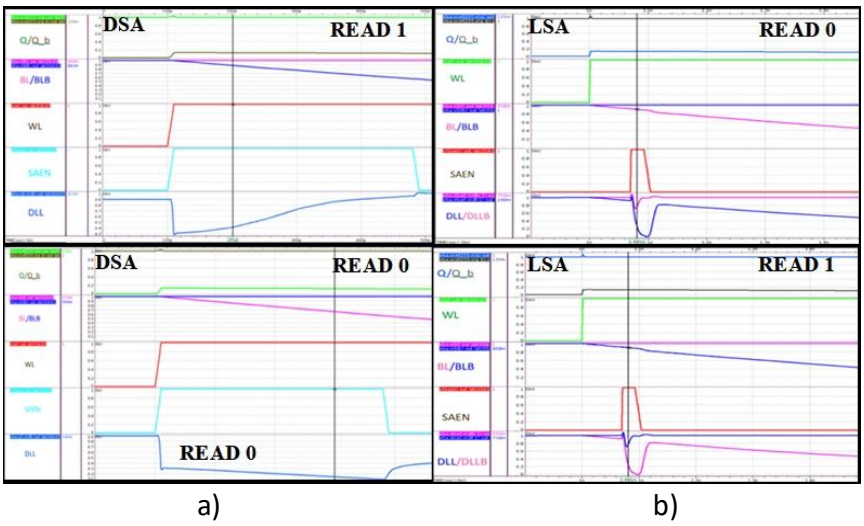


Figure 7. *The operation of reading 0 or 1 data on: a) DSA b) LSA.*

Delta V is the critical value for an optimal sense amplifier (SA) design. The Bisection method was used to find the variation of Delta V at different process corners to demonstrate that the Latch-based sense amplifier (LSA) design performs better than the Differential sense amplifier (DSA). When the voltage difference is smaller, the SA circuit can be enabled more quickly while maintaining correct functionality, resulting in faster memory read access times. Specifically, minimizing the voltage swing on the bit lines enhances the efficiency of the SA design, leading to reduced power dissipation. As shown in Figure 8, the Delta-V of LSA is 73mV, significantly lower than the 417mV of DSA at the TT corner. Therefore, the Delta V variation across different corners is much larger for the DSA compared to the LSA. This results in the DSA circuit consuming more switching voltage and causing higher dynamic power dissipation.

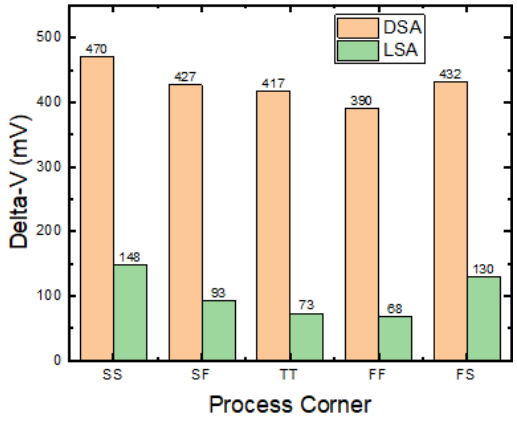


Figure 8. *Delta V for DSA and LSA.*

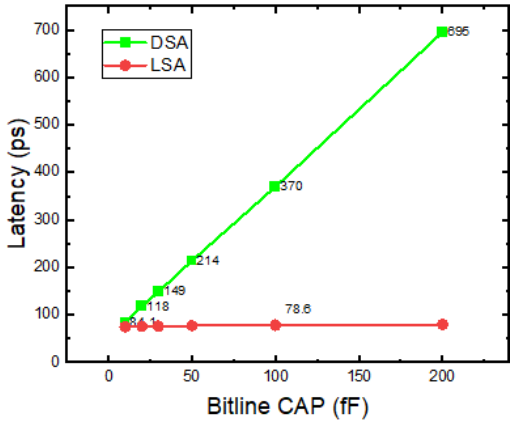


Figure 9. *The impact of capacitance on the bitline on the delay time of DSA and LSA.*

Read time is a key measure of memory cell performance. The shorter the duration from when WL is activated to when the output signal is read from the memory cell, the better the SRAM read process. Since the simulation design uses a shared bit line, the capacitance on the bit line also affects the SA's read process. Figure 9 shows that the DSA circuit is significantly affected by changes in capacitance, impacting read time. The reason for the substantial delay in the DSA circuit caused by capacitance is the need to supply a large Delta V to discharge the capacitance on the bit line. As shown in Figure 9, the LSA circuit experiences only a few picoseconds of delay variation with changing capacitance because

the LSA senses and isolates itself from the bit line. Thus, the LSA has a faster read time and is much less affected by bit line capacitance than the DSA design. Based on factors such as Delta-V and delay time, this study uses a latch-based sense amplifier design for the entire SRAM design.

The IO Block contains two data latches for input and output. Figure 10 represents the schematic diagram of the Data Input Latch which is designed based on the truth table given in Table 2. This circuit is used for latching the input data in Write operation.

Table 2. *Data Input Latch Truth Table.*

DCLK	WTI	WBI
0	DIN_b	DIN
1	Latched DIN_b	Latched DIN

Figure 11 depicts the schematic diagram of the Data Output Latch. As the name suggests, this circuit's function is to latch the data read from the Sense Amplifier. The inputs to this circuit are QT and QB, which represent the sensing bitlines after they have passed through a buffer. The output of this circuit is QOUT, which serves as the final read output of the memory. During a read operation, QT and QB will have opposite values, which will be reflected in QOUT. During a write operation, QT and QB remain high because the sensing bitlines are not discharged, causing the output to retain its previous value.

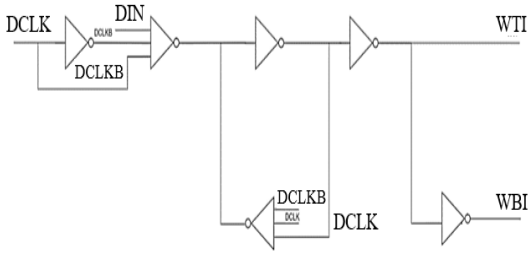


Figure 10. *Schematic Diagram of Data Input Latch.*

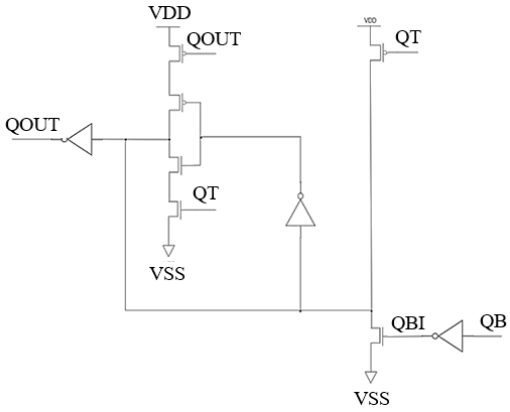


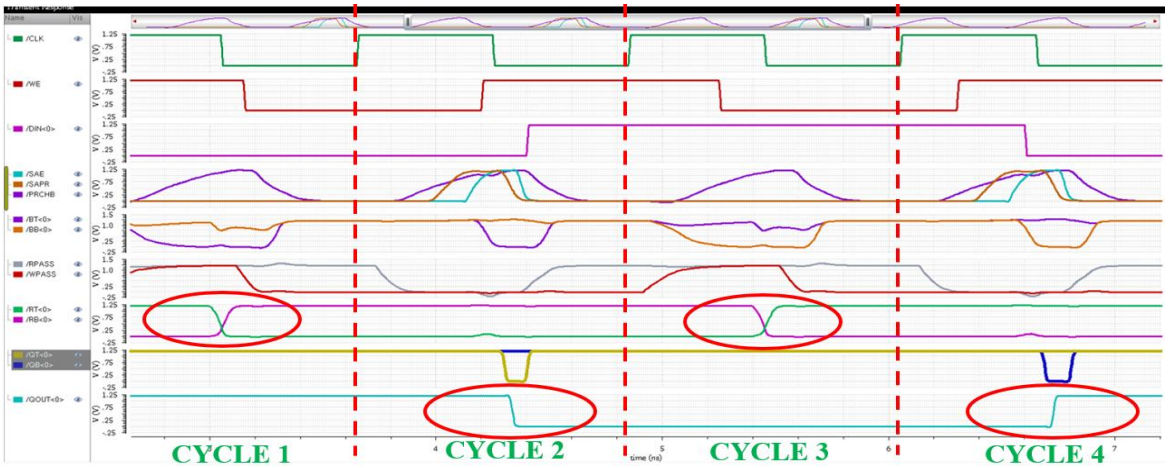
Figure 11. *Schematic Diagram of Data Output Latch.*

3.2. Results and Discussion

To validate the functionality of the proposed 8x8 SRAM design, a set of test patterns is applied. These test patterns encompass four essential inputs: CLK, WE (Write Enable), DIN<0:7> (Data Inputs), and ADR<0:2> (Address Inputs). The corresponding outputs are monitored during read and write operations. For read operations, the output is observed through QOUT<0:7>. During write operations, the data nodes of the bitcells—RT<0:7> and RB<0:7>—are scrutinized. Figure 12 illustrates the simulation results for the proposed SRAM across various read and write test cases. These results depict the waveforms of both input and output signals, as well as internal signals within the memory, providing valuable insights into its performance.

In write operations, the WE, DIN<0:7>, ADR<0:2> must be inputted before clock rises for setup time. The PRCHB signal is kept low in the low phase of clock to keep BT<0> and BB<0> at VDD level before the write operation. To enable the write function, the WE signal must be set to '1'. With WE = '1', the SA is kept inactive. When clock rises, the pre-charge is turned off by rising PRCHB, allowing the BT<0> and BB<0> to discharge. At the same time, the WCLK signal allows the decoded address to go in and trigger WL<0>. The WPASS signal is also turned on, allowing the new input data to be inserted through BT<0> and BB<0>.

In case of writing ‘0’ to the bitcell (cycle 1), the input data DIN<0> is ‘0’. With DIN<0> = ‘0’, BT<0> will quickly be pulled down as can be seen from the Figure 12. This process will flip the value stored in the bitcell, RT<0> and RB<0>. After this write operation, the value of the bitcell changes from RT<0> = ‘1’ to RT<0> = ‘0’. Hence, the write ‘0’ operation is finished successfully. Alternately, when ‘1’ is written to the bitcell (cycle 3) with the input data DIN<0> = ‘1’. For this case, the bitline bar BB<0> is pulled down instead of BT<0>. The value of RT<0> and RB<0> is flipped once again. After this write operation, the value of the bitcell changes from RT<0> = ‘0’ to RT<0> = ‘1’. Hence, data ‘1’ is successfully written into the bitcell.



Write ‘0’ into bitcells which has previous value of ‘1’at address ‘0’.
Read ‘0’ from bitcells which is previously written ‘0’at address ‘0’.
Write ‘1’ into bitcells which has previous value of ‘0’at address ‘0’.
Read ‘1’ from bitcells which is previously written ‘1’at address ‘0’.

Figure 12. *Test cases for Read and Write Operations.*

For read operation, the inputs WE and ADR<0:2> must also be inputted before clock rises for setup time. Same as the write operation, the PRCHB signal is kept low in the low phase of clock to keep BT<0> and BB<0> at VDD level before the read operation. For triggering the read operation, the write enable signal (WE) must be set to ‘0’. When clock rises, the pre-charge is turned off by rising PRCHB, allowing the BT<0> and BB<0> to discharge. Meanwhile, the RPASS is pulled low for connecting the real bitlines BT<0> and BB<0> to the Sense Amplifier. With high pulse clock and WE = ‘0’, the signal SAPR is brought high for turning off Sense Amplifier Pre-charge, which allows the sensing bitlines to mirror the behavior of the actual bitlines. When the voltage difference between the bitlines is sufficient, the Sense Amplifier enable signal SAE is switched on, allowing the values of the bitcell to be outputted.

In case of reading ‘0’ from the bitcell (cycle 2), after the precharge is turned off by switched on PRCHB, the bitlines start to discharge. The value stored in the bitcell (RT<0>) at this point is ‘0’ so BT<0> will be discharged. After that, the Sense Amplifier Pre-charge is also turned off by bringing SAPR to VDD level, which allows the voltage difference between the bitlines BT<0> and BB<0> to be mirrored. As can be seen from the figure, after the voltage of BT<0> drops to a certain amount (typically more than 20mV), the SAE signal is switched on and the values of bitlines are read out to QT<0> and QB<0> with QT<0> = ‘0’ and QB<0> = ‘1’. Then, QT<0> is latched out to output, flipping QOUT<0> value and ‘0’ can be observed at QOUT<0>. Hence, the read operation is performed successfully. Alternately, in case of read operation performed on bitcell which stores the value of ‘1’, BB<0> will be discharged after signal PRCHB being brought high and switch off the Pre-charge. Then, SAPR is also pulled up to turn off the Sense Amplifier Pre-charge. The voltage difference is sensed by the Sense Amplifier and the value stored in the bitcell will be read through QT<0> and QB<0>. In this case, BB<0> is discharged so QB<0> value is flipped to ‘0’ when SAE triggered. Hence, QT<0> is flipped

to '1' and latched out to QOUT<0>. As can be seen from the figure, '1' is observed at QOUT<0> after SAE being pulled up. This means that the read operation is finished successfully.

From the schematics and layouts of separating devices, the 8x8 SRAM memory is formed by connecting all the bitcells, the control circuit, the address decoder, the IO block and other peripheries together. All of the layouts including 8x8 Array, Address Decoder, Control Circuit, Pre-charge, Read/Write Pass Circuit, Sense Amplifier, Data Input Latch and Data Output Latch are merged and connected to each other. The metal direction rule is still applied with metal1 for horizontal signals and metal2 for vertical signals. The layout result is given in the Figure 13 and is fully verified by LVS and DRC check.

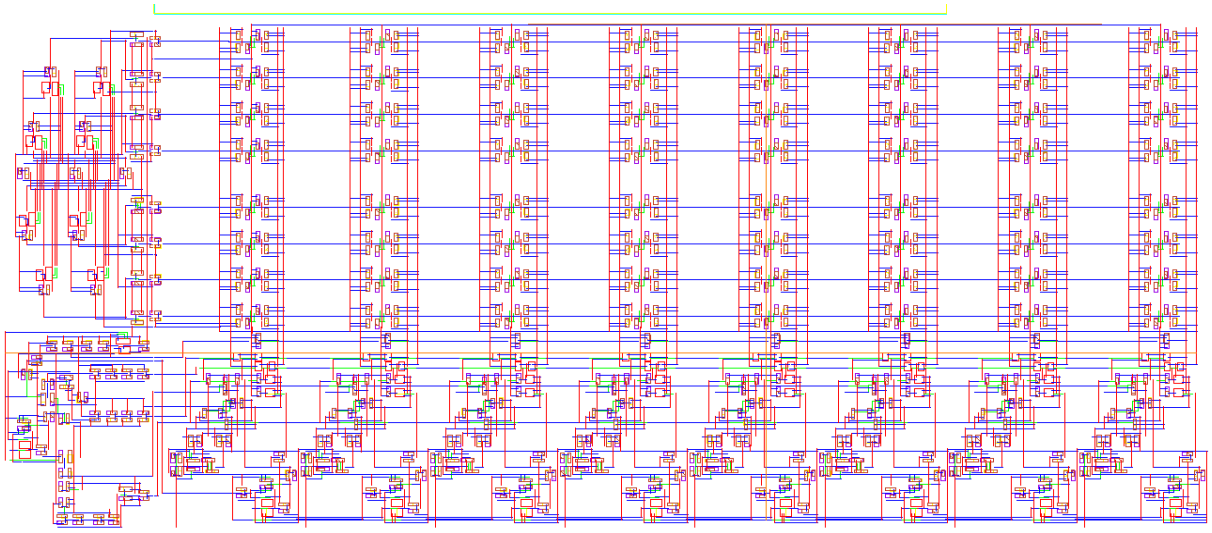


Figure 13. *64-bit SRAM Layout.*

After the read/write operations are verified by simulations, the delay of the read/write process is measured in all cases. For write operation, the delay is measured from the beginning of the operation to the point where the value stored in the bitcell flipped. With read operation, the delay is measured from the beginning of the operation to the point where the value stored in the bitcell observed at QOUT. The delay time (T_{PD}) is calculated by low-to-high delay time (T_{PDLH}) and high-to-low delay time (T_{PDHL}) and results are shown in Table 3. For worst-case scenarios, the delay is measured in case read/write operation is performed to the farthest row of bitcells.

The total power consumption of a circuit comes from the power consumed in its active state and the power consumed in its idle state as given in equation (2). The dynamic power of an SRAM memory is mostly contributed by the switching of transistors in read/write operations. Meanwhile, the power consumed in idle state is the unwanted leakage that comes from the leak currents through inactive transistors. Hence, the dynamic power is measured in case of read/write operation while the static power is measured when the memory is at idle state. The dynamic and static power is shown in Table 3. The total power consumption of the 8x8 SRAM is then calculated by equation (2): $Ptotal = 625.7 + 27.02 = 652.72\,nW$.

Table 3. *SRAM design characteristics.*

Parameters	Value	Unit
Write Delay	599.87	ps
Read Delay	677.94	ps
Dynamic Power	625.70	nW
Static Power	27.02	nW
Peak Current	2.23	mA

4. Conclusions

In this paper, a complete 64-bit SRAM design is realized using a 6T configuration for the memory cells and a latch-based sense amplifier. The SRAM is organized into 8 words, each consisting of 8 bits. Comprehensive testing is conducted to thoroughly evaluate the memory operation, as illustrated by the timing diagrams. Both static and dynamic power dissipation of the memory are measured and analyzed. The memory layout is created, with each component verified through Design Rule Check (DRC) and Layout Versus Schematic (LVS) checks using Assura. The design features a single set of peripherals shared by eight bitcells in the same column, leading to significant reductions in memory size and power consumption. Additionally, the layout is optimized for area, symmetry, and adherence to metal rules.

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Conflict of Interest

The authors declare that they have no competing interests.

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